HIGH SPEED SIGNAL PROCESSING APPLICATIONS
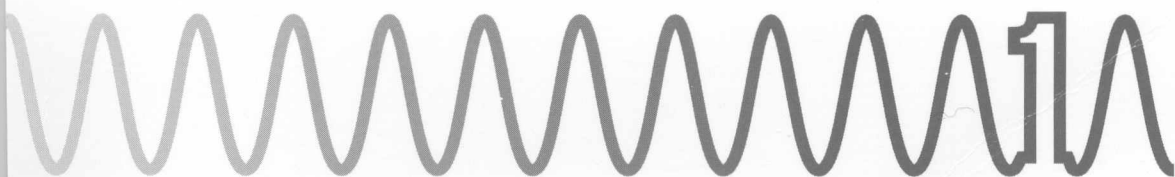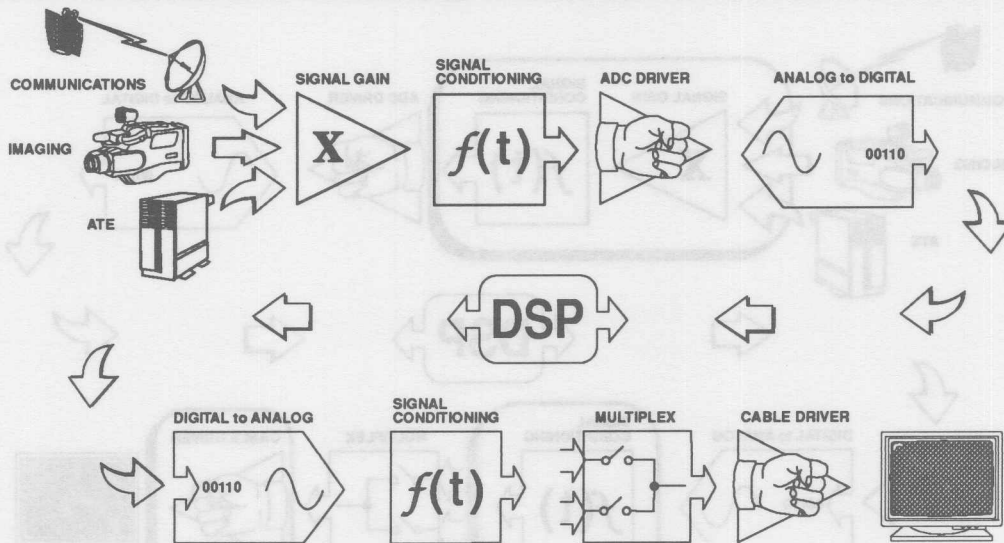
HARRIS
SEMICONDUCTOR

**Harris Semiconductor
High Speed Signal Processing Seminar**

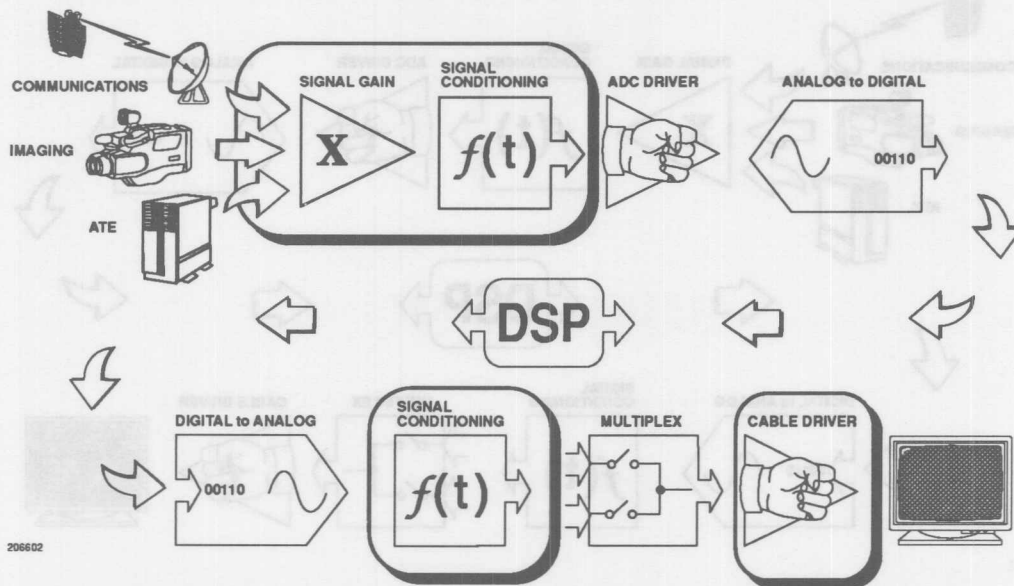206601

High Speed
Signal Processing
Seminar

1992

Section 1 - Signal Conditioning and Buffering
Section 2 - Data Conversion
Section 3 - Digital Signal Processing
Section 4 - Video/Imaging Demonstration

Harris Semiconductor

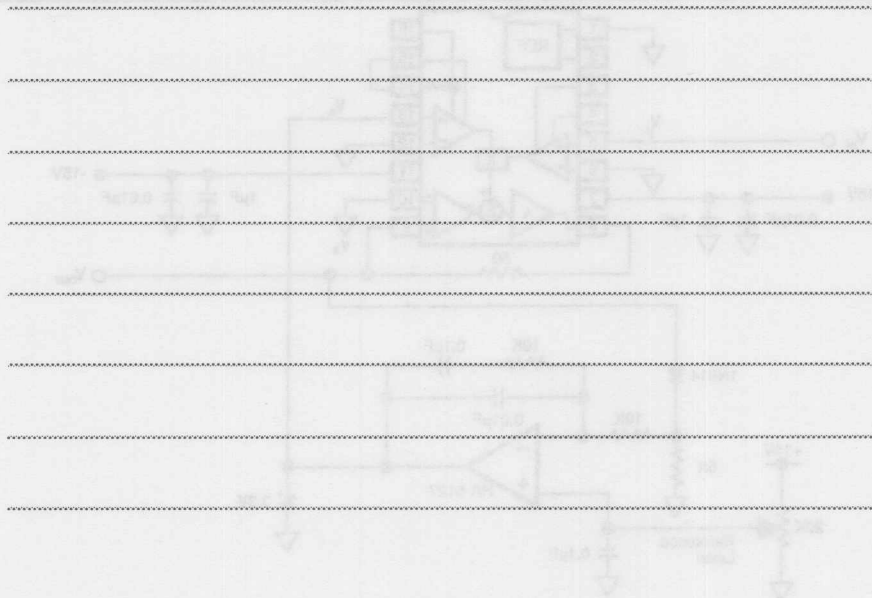COMMUNICATIONS

IMAGING

ATE

SIGNAL GAIN

X

SIGNAL CONDITIONING

$f(t)$

ADC DRIVER

ANALOG to DIGITAL

00110

DSP

DIGITAL to ANALOG

00110

SIGNAL CONDITIONING

$f(t)$

MULTIPLEX

CABLE DRIVER

206602

SIGNAL CONDITIONING

AND

BUFFERING

3

System Gain and Offset Adjust

• GAIN AND OFFSET ADJUST ARE DONE TO:

  - Size the Analog Input Signal for Maximum Resolution Through the ADC

  - Provide a Reference with Which to Judge the Data

• WHERE TO ADJUST

- The Computer Processor?	Easily Done but You Lose ADC Resolution
- The ADC?	May Introduce Unnecessary Distortion
- The ADC Driver?	No Gain Adjust Here
- The Signal Gain Stage?	Can't Afford to Sacrifice Bandwidth Here
- Signal Conditioning	Gain and Offset Can be Adjusted with an AUTOMATIC GAIN CONTROL (AGC) Circuit Here

206604

## Automatic Gain Control Using HA-2546

206605

4
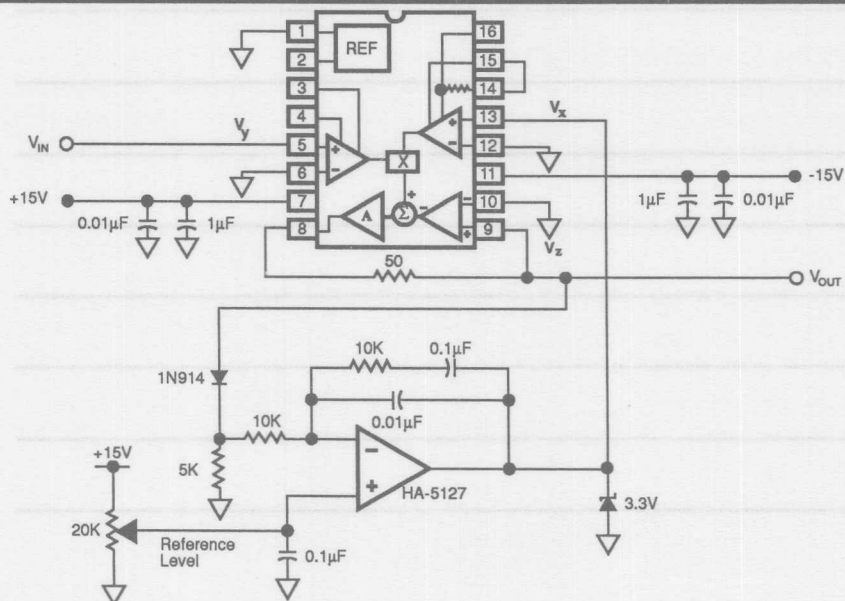
Several options exist with respect to when and where to condition an incoming signal.

We can decide not to condition the analog signal at all, and adjust the scaling and offset after the data has been converted into digital. Certainly the math is not difficult, but you cannot do the math on data you don't have. If the signal is being clipped by the limited range of the ADC or the data only uses a fraction of the digital codes available, distortion and lost resolution result.

Adjusting the Full Scale Reference and Offset of the ADC can help, but excessive changes will alter the designed operating point for the ADC. The linearity of the ADC will suffer. The datasheet specifications only hold for the stated operating conditions, deviate from them at your peril.

The ADC driver, usually a high frequency buffer, concentrates on the job of providing a low source impedance and doesn't have the features needed for Gain and Offset adjustment.

The multiplier is configured for a true Automatic Gain Control or AGC application here. The HA-2546 low noise op amp provides the gain control level to the X input. This level will set the peak output voltage of the multiplier to match the Reference Level. The feedback network around the HA-2546 provides stability and a response time adjustment for the gain control circuit. Also notice that the signal bandwidth is not affected by the gain signal (Vx) as it can be in other AGC circuits.
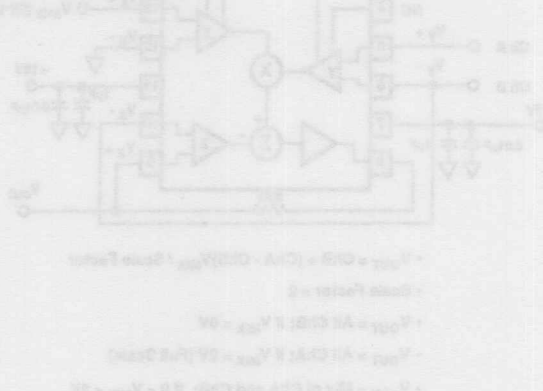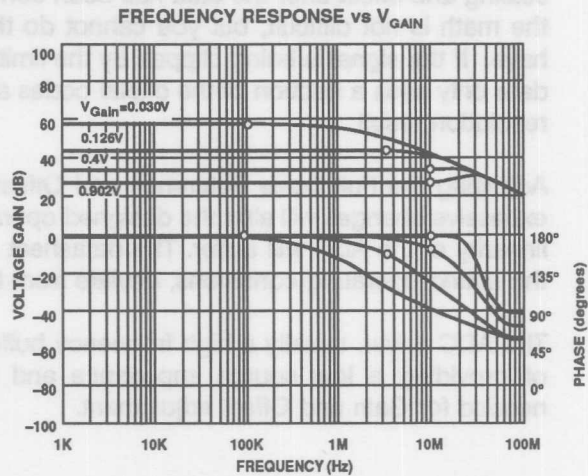
HA-2546 Voltage Controlled Amplifier

FREQUENCY RESPONSE vs V_{GAIN}
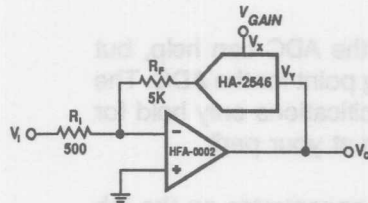
206606

Video Fader Using HA-2546
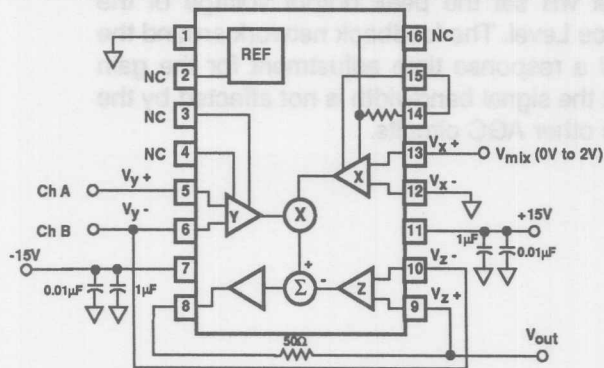
- V_{OUT} = ChB + (ChA - ChB)V_{MIX} / Scale Factor
- Scale Factor = 2
- V_{OUT} = All ChB; if V_{MIX} = 0V
- V_{OUT} = All ChA; if V_{MIX} = 2V (Full Scale)
- V_{OUT} = Mix of ChA and ChB; if 0 < V_{MIX} < 2V

206607

"Dial" in the gain of your circuit with this Voltage Controlled Amplifier. As Vgain is reduced from its Full Scale value, the feedback is attenuated thus creating a higher forward gain. Here the gain is swept from 20V/V with Vgain=0.902V to a gain of almost 1000V/V with Vgain=0.03V. The full dynamic range of wideband amplifiers can now be brought to bear, without resorting to switched discrete ranges.

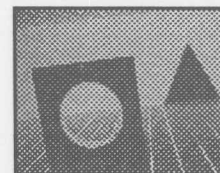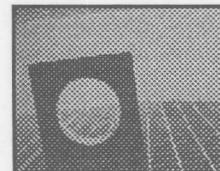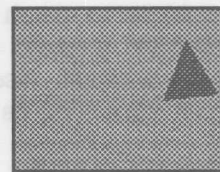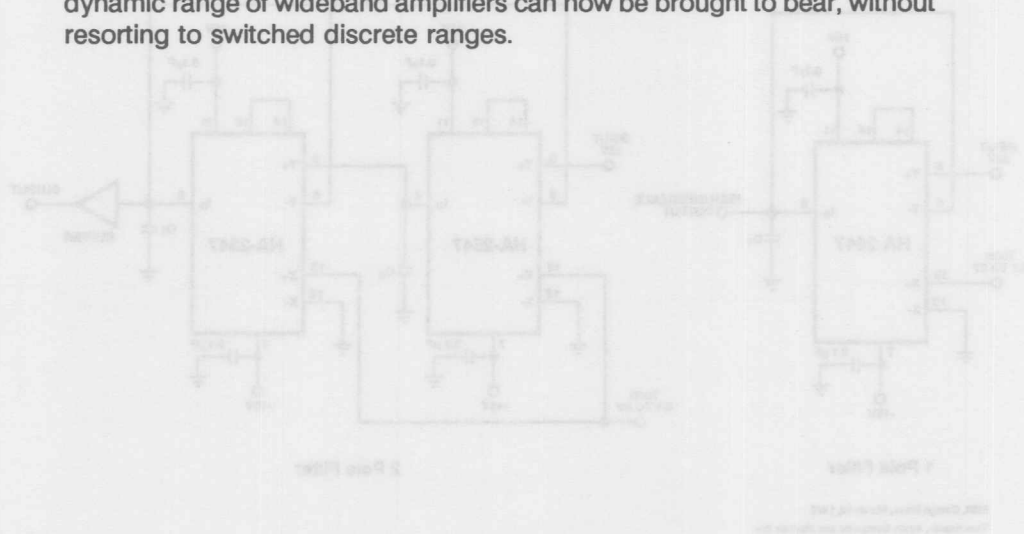The Video Fader circuit provides a unique function. Here Ch B is applied to the inverting Z input in addition to the inverting Y input. In this way, the function [Vout=Ch B + (Ch A - Ch B)Vmix/ScaleFactor] is generated. Vmix will control the percentage of Ch A and Ch B that are mixed together to produce a resulting image.

In the case that Vmix=0V, the transfer equation becomes Vout=Ch B. Conversely, when Vmix is at its Full Scale value, equal to the Scale Factor, the equation becomes Vout=Ch B + (Ch A - Ch B) which equals Vout=Ch A. Values of Vmix in between will result in a blending of Ch A and Ch B.

HARRIS
SEMICONDUCTOR
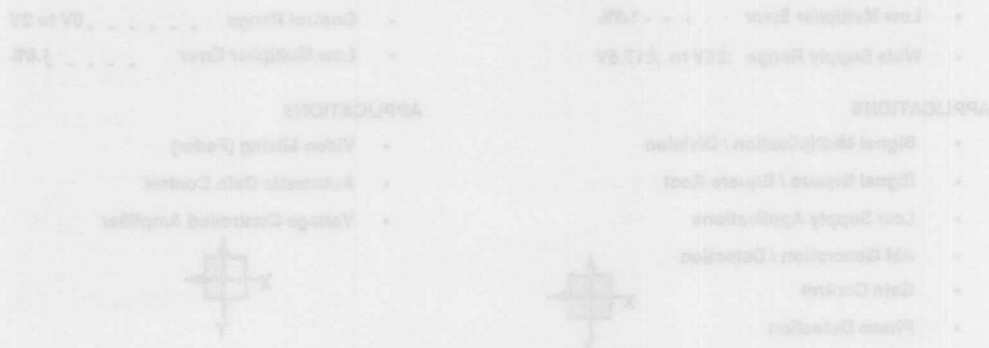
Tunable Filters Using HA-2547s
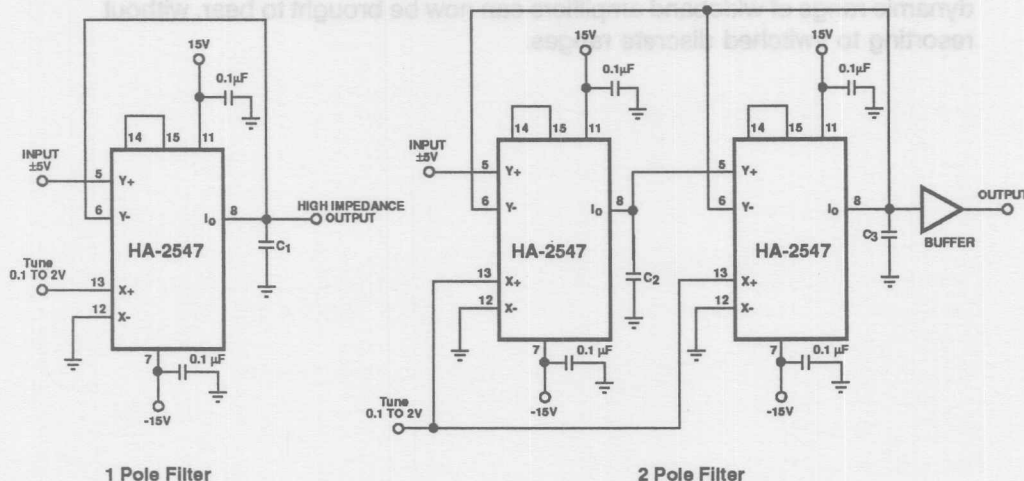
1 Pole Filter

2 Pole Filter

---

4 Quadrant Multiplier vs 2 Quadrant Multiplier

HA-2556	HA-2546
4 Quadrant Multiplier	2 Quadrant Multiplier

FEATURES

- Wide Signal Bandwidth . . . - 30MHz
- Matched X, Y, Z Channel Bandwidth
- High Slew Rate 350V/μs
- Differential Input Range . . . $\pm$5V
- Low Multiplier Error 1.5%
- Wide Supply Range $\pm$5V to $\pm$17.5V

APPLICATIONS

- Signal Multiplication / Division
- Signal Square / Square Root
- Low Supply Applications
- AM Generation / Detection
- Gain Control
- Phase Detection

FEATURES

- Wide Signal Bandwidth . . . 30MHz
- Control Bandwidth 17MHz
- High Slew Rate 300V/μs
- Signal Range . . . . $\pm$5V
- Control Range . . . . . . 0V to 2V
- Low Multiplier Error 1.6%

APPLICATIONS

- Video Mixing (Fader)
- Automatic Gain Control
- Voltage Controlled Amplifier

206609

8
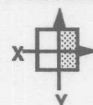
The HA-2547 current output multiplier has a 100MHz signal bandwidth. Since there is no output voltage gain stage, loop feedback is not required. Instead, the HA-2547 provides a fixed transconductance of about 200 micro-mhos or 1/5000 ohm (Scale Factor = 2). The transfer equation is simple, compared to its voltage output cousin: Iout=XY/(2500*SF).

A tunable filter results when a pole capacitor is added to the output to convert Iout into a voltage and the output is fedback to the inverting Y input. The node equations are:

1) Vout = ZcX(Ypos - Yneg)/5000; where Zc is output capacitor impedance and SF = 2.
2) Vin = Ypos
3) Yneg = Vout.

By substituting equations 2 and 3 into equation 1 and solving for Vout/Vin, the transfer function becomes: Vout/Vin = 1/(1 + 5000/XZc). This is a single pole low pass filter with the -3dB frequency occurring where XZc = 5000. If you set Zc = 1/(2*3.14*F*20pf) and we adjust X from 0.1V to 2V, the pole frequency will move from 159KHz to 3.18MHz. Similarly, the two pole filter expands on this idea but providing twice the reject-band rolloff. For a Butterworth response, C2 should be twice C3. These tunable filters are able to achieve stopband attenuations of over 30dB. When selecting an output capacitor value, take into account 6.5pf of output capacitance, 2.5pf of input capacitance plus any other circuit related parasitics.

Up until now, we have looked at 2 quadrant multipliers. These devices have a bipolar (+/-5V) wideband (30MHz) signal input and a somewhat slower (17MHz) unipolar (0V to 2V) control input. Multipliers of this variety are useful for AGC type applications, or any application using a relatively slow control voltage to operate on an incoming signal.

In contrast, the 4 quadrant multipliers, the HA-2556 and the HA-2557, feature matched input characteristics for X, Y and Z. This is useful in applications that require a wideband bipolar signal be applied to separate inputs, such as in Synchronous AM Detection or Phase Detection. Additionally, 4 quadrant multipliers are still an excellent choice for AGC or control type applications. You may review additional multiplier circuit configurations and applications in this handout.
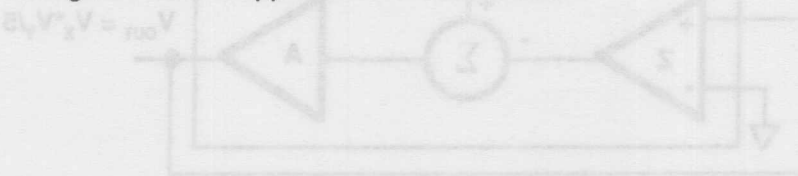
HA-2556/57
Wideband Four Quadrant Multipliers

- **FEATURES**
  - **Low Multiplication Error of 1.5%**
  - **30/100MHz Signal Bandwidth**
  - **0.1% Differential Gain**
  - **0.1° Differential Phase**
  - **0.1dB Gain Flatness to 10MHz**
  - **350V/µs Slew Rate (HA-2556)**
  - **5µA Bias Current**
  - **Improved Version of the MPY600**

206610

Analog Multiplier Applications

Multiplication

$V_{OUT} = V_X * V_Y / 5$

206610A

Scale Factor is inherent to Component.
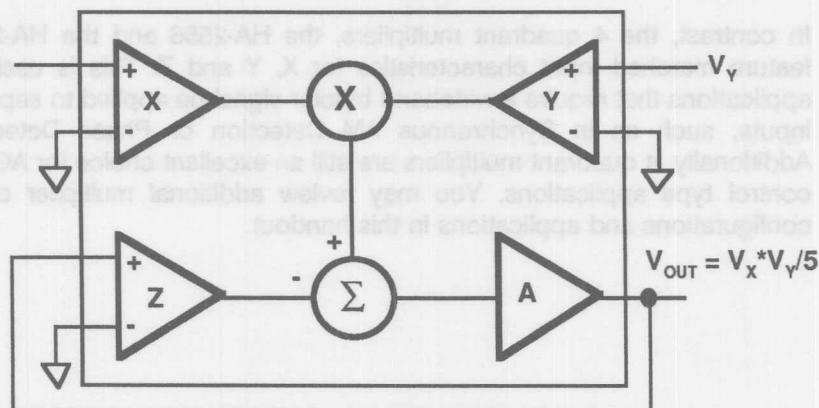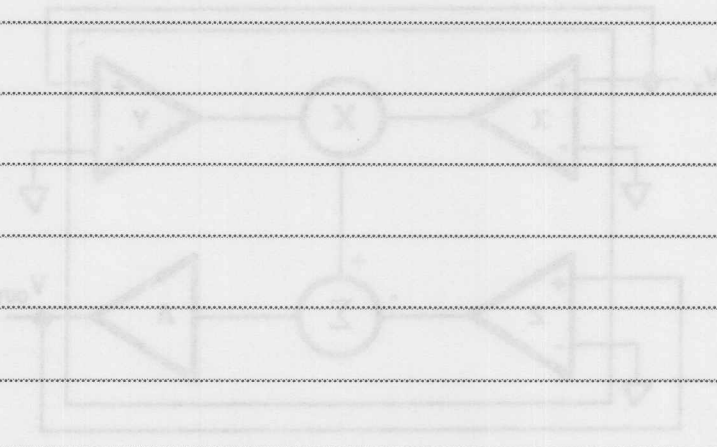
Analog Multiplier Applications

Division

$V_{OUT} = 5V_Z/V_X$
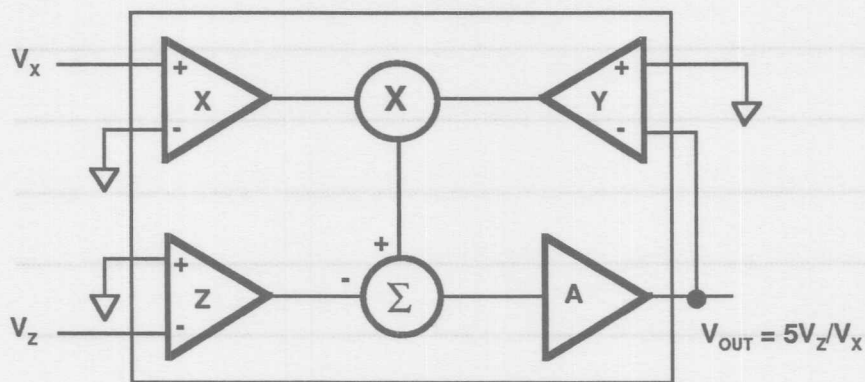
$V_X > 0V$ TO AVOID POSITIVE FEEDBACK

206610B

Analog Multiplier Applications

Squarer

$V_{OUT} = V_X^2/5$
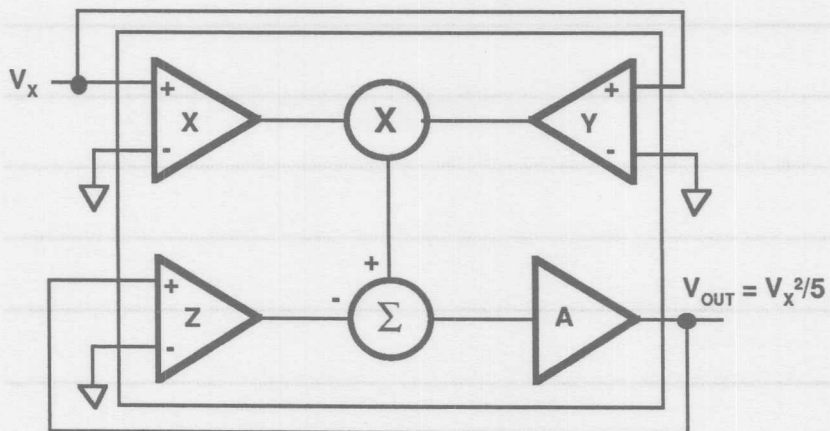
206610C

Analog Multiplier Applications

Square Root

$$V_{OUT} = (5V_Z)^{1/2}$$
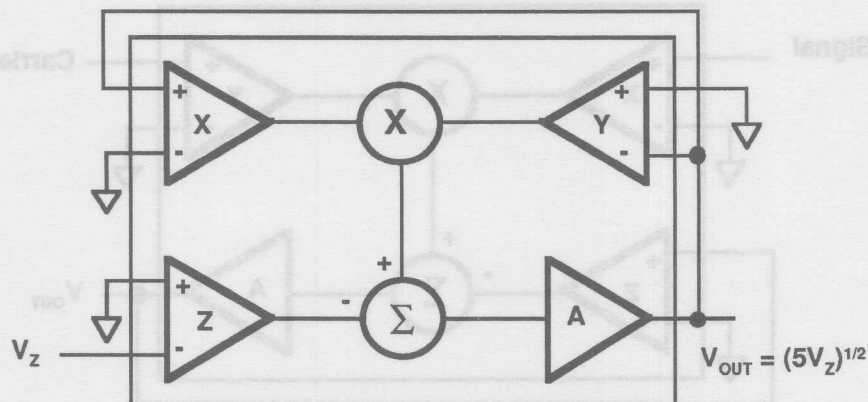
$V_Z > 0V$ TO AVOID POSITIVE FEEDBACK

206610D

Analog Multiplier Applications

AM Signal Generation

$AC_{OS}(W_At)$

$CC_{OS}(W_Ct)$
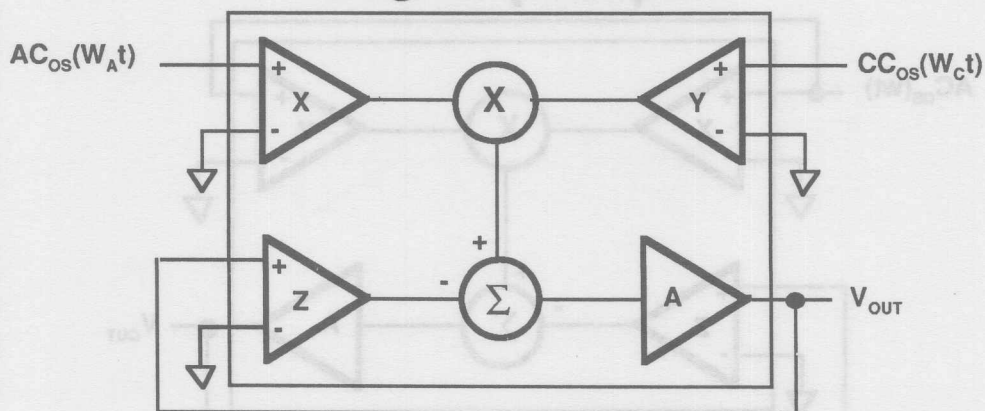
V_{OUT}

$$V_{OUT} = (AC/10)(C_{OS}(W_C-W_A)t + C_{OS}(W_C+W_A)t)$$

206610E

Analog Multiplier Applications

Synchronous AM Detection

AM Signal ... X ... Carrier

X Y

Z Σ A ... V_OUT
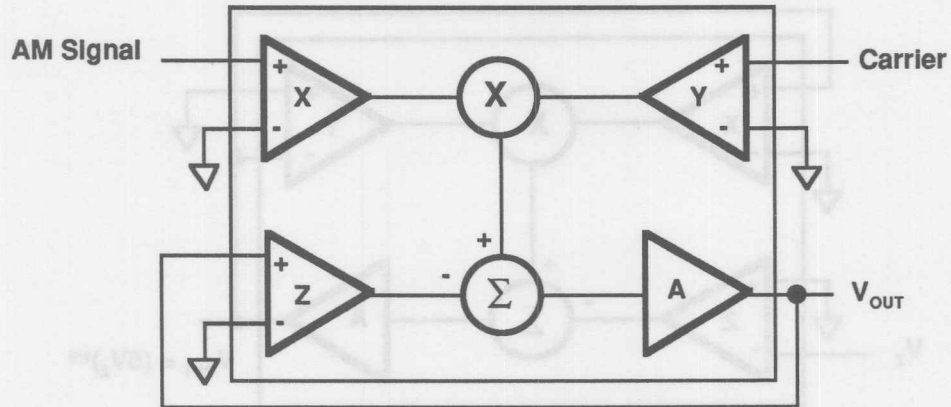
**LIKE FREQUENCY DOUBLER YOU GET
AUDIO CENTERED AT DC AND 2Fc**

206610F

Analog Multiplier Applications

Frequency Doubler

$AC_{os}(wt)$

X Y

X

Z Σ A ... V_OUT
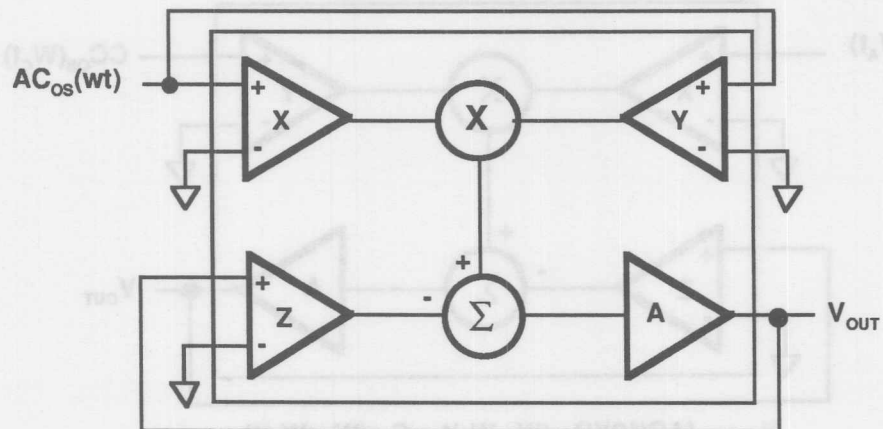
$$V_{OUT} = (A^2/10)(1+C_{os}(2wt))$$

206610G

Analog Multiplier Applications

Phase Detection

$AC_{OS}(wt)$ — [X] — (X) — [Y] — $AC_{OS}(wt+\emptyset)$

[Z] — (Σ) — [A] — V_{OUT}
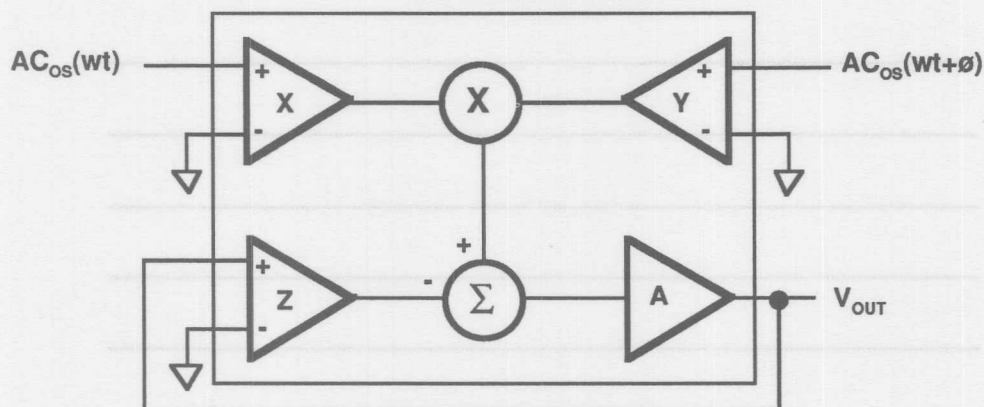
$$V_{OUT} = (A^2/10)(C_{OS}(\emptyset) + C_{OS}(2wt))$$

206610H

DC COMPONENT IS PROPORTIONAL TO $C_{OS}(\emptyset)$

Current Feedback Amplifiers

BLOCK DIAGRAM

$+I_{BIAS}$ +IN +1 OUT O V_{out}

V_{IN}

$-I_{BIAS}$ -IN R_I i_e R_H C_H +1

R_F

R_G
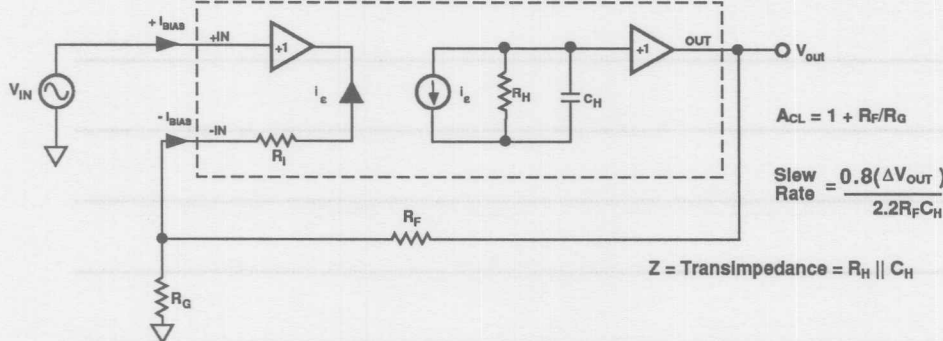
$A_{CL} = 1 + R_F/R_G$

$$\text{Slew Rate} = \frac{0.8(\Delta V_{OUT})}{2.2 R_F C_H}$$

$Z = \text{Transimpedance} = R_H \parallel C_H$

- **IDEAL OP AMP ASSUMPTIONS STILL HOLD:**
  1. $V_{-IN} = V_{+IN}$; Input Buffer Forces -IN to Follow +IN
  2. $+I_{BIAS} = 0$; Input Buffer has High Input Impedance
  3. $-I_{BIAS} = 0$; $-I_{BIAS} = i_e$, $V_{OUT} = Zi_e$, Z is Large so i_e is Small During DC Operation

206611

Current Feedback (CFB) Amplifiers differ from Voltage Feedback (VFB) Amplifiers in that the error signal fed back to the input stage is a current rather than a voltage. A high input impedance buffer drives the -Input to the same potential as the +Input. When an input transition occurs, this input buffer sources or sinks current to maintain a near zero potential difference between the inputs. The -Input current is mirrored onto a high impedance node, for conversion to a voltage via the amplifier's transimpedance gain, Z. Another unity gain amplifier buffers the output to provide drive and load insensitivity. The feedback loop keeps the output voltage changing, until the error current is minimized. During steady state, only a small DC current (defined by V_{OUT}/Z) flows through the -Input.

The input buffer's low output impedance allows large currents to flow through the -Input. Because this current is the slewing current, the slew rate is extremely large, and is a function of R_F and the change in V_{OUT}. The dependence on ΔV_{OUT} gives the CFB amplifier the novel feature of nearly constant output transition times, regardless of step size. R_F and C_H set the transition time, so the output has an exponential shape with time constant $R_F C_H$, and the 10% to 90% transition requires 2.2 time constants.

Frequency Response of Current Feedback Amplifiers

- IDEAL CURRENT FEEDBACK AMP ($R_I = 0$) TRANSFER FUNCTION:

$$A(jf) = \frac{A_{CL}}{1 + j(2\pi f R_F C_H)} \qquad \text{and } A_{-3dB} \text{ occurs at} \qquad f = f_{-3dB} = \frac{1}{2\pi R_F C_H}$$

- FOR A FINITE R_I, THE BW EQUATION BECOMES:

$$f_{-3dB} = \frac{1}{2\pi C_H (R_F + A_{CL} R_I)} \qquad \text{where } R_F \text{ is modified by the BW reducing term } A_{CL} R_I$$

- THE BW REDUCTION AT HIGHER A_{CL} CAN BE COMPENSATED BY REDUCING THE R_F ACCORDING TO THE FOLLOWING EQUATION:

$$R_f' = R_f - A_{CL} R_I$$

206612

Gain Bandwidth Product Advantage of Current Feedback Amplifiers

$$\text{BW (@ } A_{CL} > 1) = 100\text{MHz} \frac{R_F}{R_F + A_{CL} R_I}$$

$$\text{BW (@ } A_{CL} > 1) = 300\text{MHz} \frac{1}{A_{CL}}$$
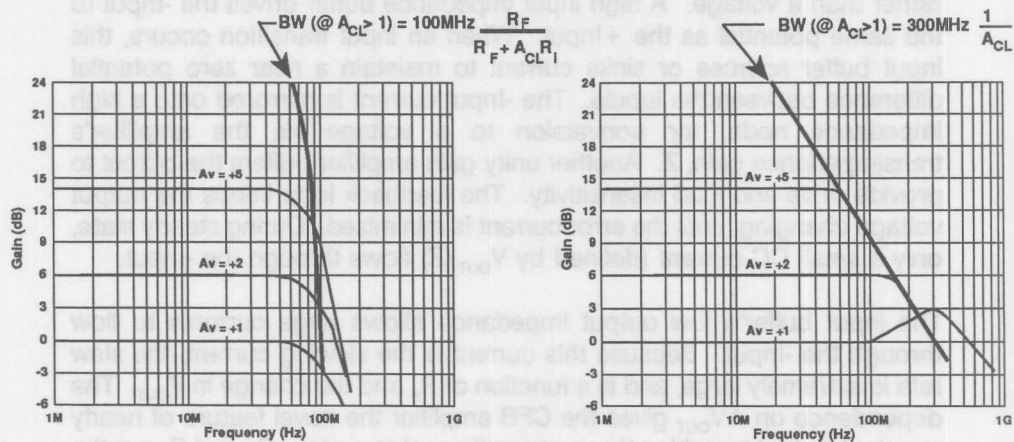
HA-5004 CFB Amp. ($R_F = 250\Omega$)

HFA-0005 VFB Amp.

206613

18

Starting with the standard op amp gain equation, and realizing that the loop gain of a CFB Amplifier is the ratio of the open loop transimpedance (Z) to R_F, allows the development of the transfer function for the ideal CFB amplifier. The equation for f_{-3dB} shows that the bandwidth is predominantly set by R_F and the capacitance at the high impedance node, C_H. Note that bandwidth has no dependance on R_G. Thus, closed loop gain adjustments, via R_G changes, have no affect on bandwidth.

Another observation is that bandwidth is inversely proportional to R_F, indicating amplifier gain shouldn't be set by varying R_F. CFB amplifiers require R_F even in unity gain configurations. If $R_F = 0$, the amplifier has infinite bandwidth and would obviously be unstable. A similar argument precludes the use of feedback capacitors, due to the reduction in the effective R_F at high frequencies.

A practical CFB amplifier has a finite R_i that impacts the transfer function by reducing the loop gain. As the closed loop gain increases, R_i becomes more of a factor in setting the bandwidth. This effect is not as severe as the gain bandwidth product limitation of VFB amplifiers. The bandwidth decrease can be compensated by reducing R_F at gains greater than 1.

Because CFB amplifiers are relatively independent of closed loop gain, the term Gain Bandwidth Product (GBWP) isn't applicable. An ideal CFB amplifier would have constant bandwidth at any gain, for a theoretically infinite GBWP. The graphs shown here illustrate both the GBWP limit of a VFB amplifier, and the gain insensitivity of a CFB amplifier. Although the Unity Gain Bandwidth of the HFA-0005 is three times that of the HA-5004, the CFB amplifier surpasses the 0005 (88Mhz vs. 70MHz) at a gain of just five. The very low R_i (6.5Ω) of the HA-5004 results in a nearly ideal gain vs. bandwidth response.

Comparison of Current and Voltage Feedback Amplifiers

ADVANTAGES OF CFB AMPLIFIERS

- BW is More Constant Over a Wide Range of A_{CL}

- R_F Changes Can Compensate for BW Reductions Due to R_L, A_{CL}, etc.

- Noise BW Can be Reduced by Increasing R_F, Which Eliminates C_F

- Virtually No Slew Rate Limiting

- Low Distortion Due to Better Large Signal Behavior

- Fast Settling Characteristics

206614

ADVANTAGES OF VFB AMPLIFIERS

- Drives Capacitive Feedback (Filters, Integrators) and Loads

- R_F Not Required for Unity Gain Applications

- Low Noise Amplifiers Available

- Wide Range of Specialized Choices (Choppers, Precision, etc.)

- Symmetrical Bias Currents Allow Source Impedance Matching to Minimize Offset Errors

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Harris Current Feedback Amplifiers

DEVICE	DESCRIPTION
HA-5004	$A_V \geq 1$; 100MHz; Thermal Overload Protected
HA-5020	$A_V \geq 1$; 100MHz; Lower Cost, Enhanced EL2020 Replacement
HFA1100	$A_V \geq 1$; 850MHz; SR = 2500V/μs; On-Chip Output Clamping for Fast (10ns) Overdrive Recovery
HFA1120	$A_V \geq 1$; 850MHz; HFA1100 with Offset Adjust
HFA1130	$A_V \geq 1$; 850MHz; HFA1100 with Programmable Output Clamps, 750ps Overdrive Recovery Time
HFA1110	Unity Gain Closed Loop Buffer; 850MHz; Industry Standard Buffer Pinout
HFA1112	Programmable Gain (A_V = +2, +1, -1) Closed Loop Buffer; 850MHz; Standard Op Amp Pinout

IN
0 to 0.5V

OUT
0 to 1V
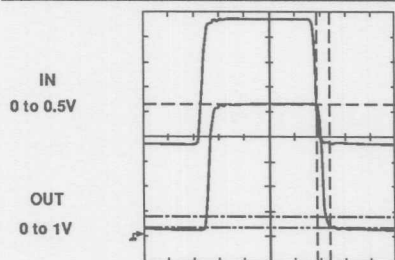
HFA1130 Unclamped Pulse Response
(A_V= +2)

IN
0 to 1V

OUT
0 to 1V

Timebase = 10ns/Div
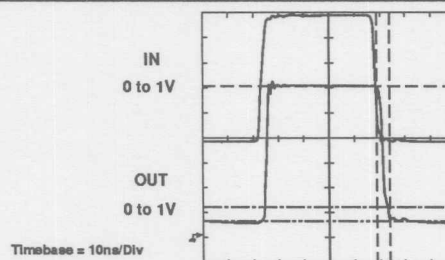
HFA1130 Clamped Pulse Response
Clamps = ±1V (A_V = +2)

206615

With all this talk about CFB amplifiers, why would anyone use VFB amplifiers anymore? Both amplifier types have advantages. CFB amplifiers have speed and flexibility advantages, making them the new dominant force in high speed circuits. Wide bandwidths and amazing slew rates yield sub-nanosecond output transitions, several nanosecond settling times, and low distortion at high output power. If a design ends up a little shy on bandwidth, a simple R_F tweak can boost it. Additionally, a design might use one CFB amplifier type in four gain configurations that would otherwise require four different VFB amplifiers. But CFB amplifiers are harder to work with due to their sensitivity to stray capacitances.

VFB amplifiers remain the workhorse in the industry. With millions of proven applications, they are well understood by analog designers. They lend themselves to straightforward filter and integrator designs, and are the best choice for low noise and precision applications.

Harris offers a broad selection of CFB devices, including the world's fastest amplifier, and a novel programmable gain buffer in a standard op amp pinout. This one buffer satisfies applications requiring gains of +1, -1 or 2. The standard amplifier pinout allows the buffer to drop into low gain op amp sockets, to save resistors or increase performance.

The scope plots at the bottom of the slide illustrate the subnanosecond overdrive recovery time of the HFA1130. The difference between the clamped and unclamped propagation delays is the recovery time. The measurement uses the 90% point of the output transition, to ensure that true linear operation has resumed. In the plots shown, the unclamped propagation delay is 4.0ns, while the clamped (2X overdrive) propagation delay is 4.8ns.

Note: The propagation delay illustrated is dominated by the delay through the fixturing and cables. The typical propagation delay of HFA11XX devices is 500ps.

Superior Gain Flatness Requires Very Wide Bandwidth

Minimum f_{-3dB} for $\pm0.1dB$ Gain Flatness to 50MHz (based on single pole model):

$$f_{-3dB} \geq \sqrt{\frac{f_{flat}^2}{\left(\frac{1}{0.989}\right)^2 - 1}} \quad \text{where } 0.989 = 10^{(-0.1dB/20)}, \text{ and } f_{-3dB} = BW \text{ at } A_{CL} \text{ of interest}$$

$$\geq 334MHz \quad \text{which implies a typical BW of 500 - 700MHz}$$
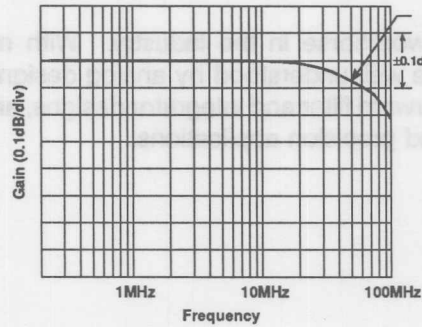
HFA1100
$A_V = +2$
Gain Flatness < 0.1dB to 50MHz

50MHz
$\pm0.1dB$

Gain (0.1dB/div)

1MHz   10MHz   100MHz
Frequency

206616

Phase Linearity Also Requires Very Wide Bandwidth

HFA1100 Deviation from Linear Phase

100MHz

±0.5 degree

0

DLP (0.5deg/div)

0MHz   75MHz   150MHz
Frequency

206617

22
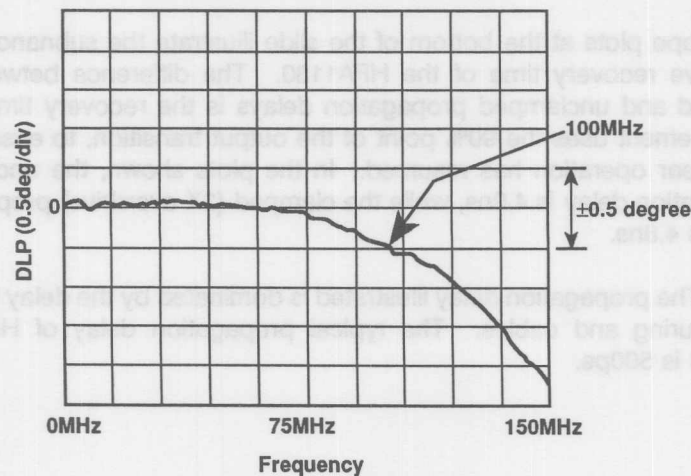
Gain flatness (or frequency distortion) is one type of linear distortion that is important in many applications. If the gain varies over the frequency band of interest, different frequencies receive different amplifications, and signal distortion results.

The equation shows that gain flatness is a function of the amplifier's -3dB frequency. A flatness requirement of ±0.1dB to 50MHz requires a -3dB bandwidth in excess of 334MHz. With a common variability of 1.5 or 2 to 1, this equates to a typical bandwidth of 500-700MHz.
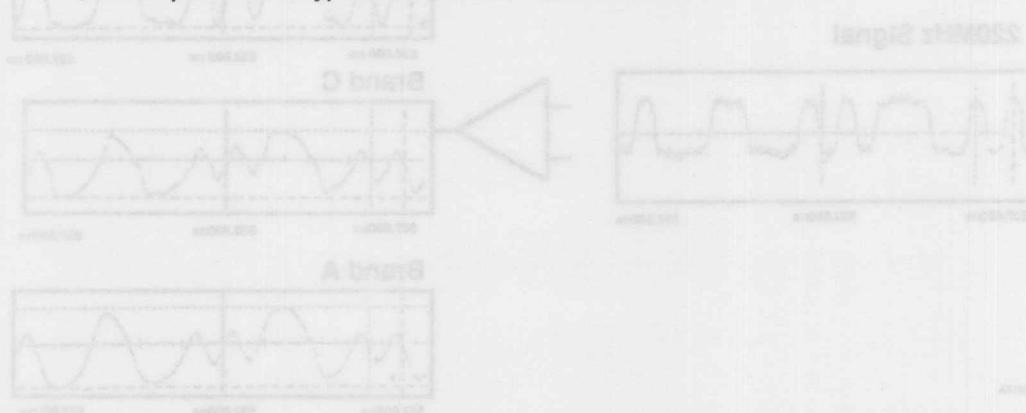
A second type of linear distortion is non-linear phase shift. An ideal op-amp would have zero phase shift over its entire frequency range. Because this is impractical, a realistic goal is phase shift that is proportional to frequency. This results in a constant time delay through the amplifier at any frequency. Phase linearity is the term that indicates a phase shift proportional to frequency. Deviation from Linear Phase (DLP, in degrees) indicates the maximum difference between the actual phase shift, and the desired linear phase shift.

In most cases wider bandwidth amplifiers deliver better phase linearity. For a single pole amplifier, obtaining a 100MHz DLP of 0.5 degrees or less requires a minimum -3dB bandwidth of 334MHz. Again, this translates to a typical bandwidth of 500-700MHz.
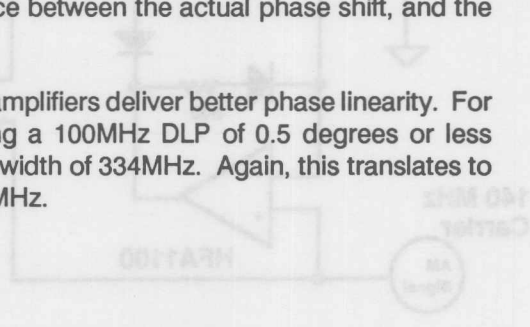
Which Amplifier Would You Choose?

OUTPUT ($A_V = 2$)

INPUT

HFA1100 Op Amp

220MHz Signal

507.800 ns   532.800 ns   557.800 ns

507.800ns   532.800ns   557.800ns

Brand C

507.800ns   532.800ns   557.800ns

Brand A

507.800ns   532.800ns   557.800ns
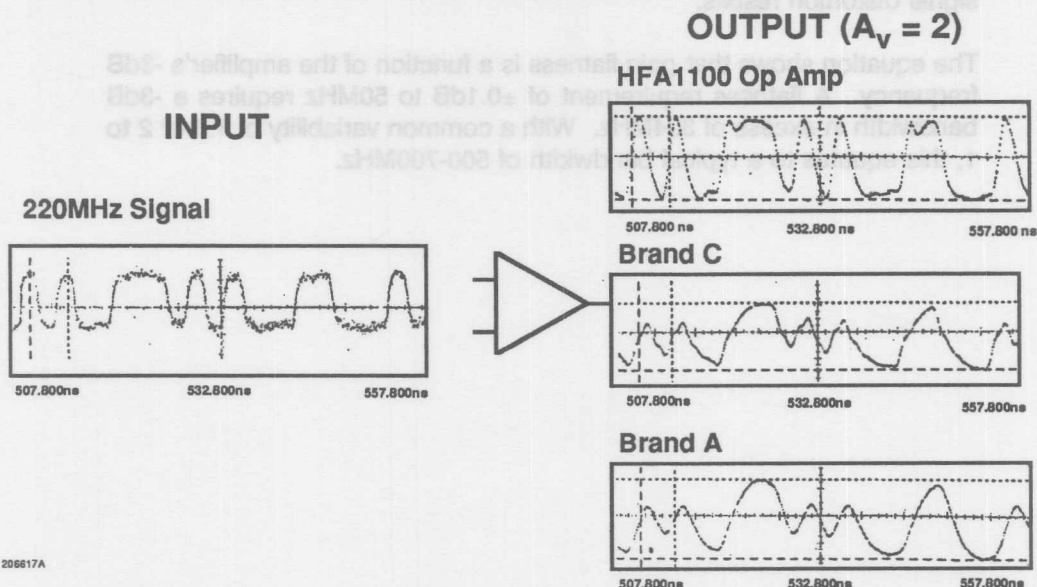
206617A

High Input Impedance
Full Wave Rectifier - AM Demodulator

500   500   250   500

HFA1100

Low
Pass
Filter

V_{OUT}

**140 MHz
Carrier**

500

AM
Signal

HFA1100
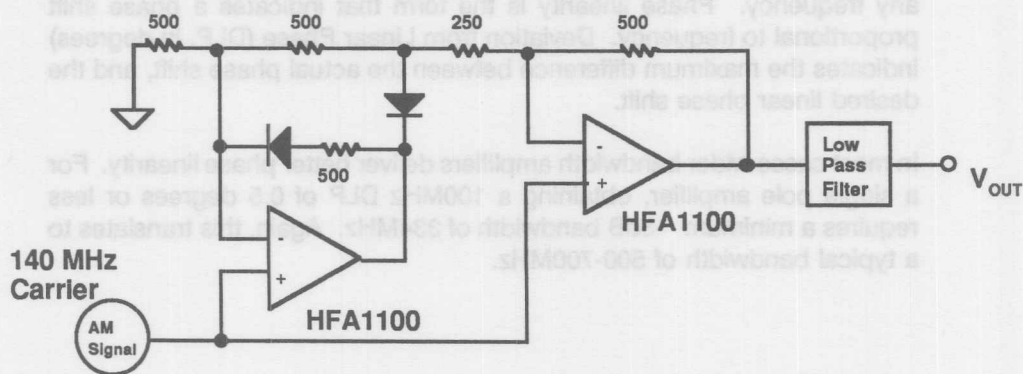
V_{out} **Swing Is Limited To 1/2 V_{out}
Range Due To 1st AMP Gain + 2.**

206617B

24

Differential Gain and Phase

WHAT IS IT?

- Variations in an Amplifier's Small Signal Gain and Phase Response at the Chrominance (Color) Frequency Due to Changes in the Luminance (Brightness) Level.
- Differential Gain (DG) is Expressed as the Percentage of Chrominance Amplitude Variation of an Amplifier's Output due to Changes in the Luminance Level.
- Differential Phase (DP) is Expressed as the Difference in the Chrominance Phase Shift (in Degrees) of the Amplifier Output at Two Different Luminance Levels.

WHAT PROBLEMS DOES IT CAUSE?

- DG Distortion Appears as Variations in Color Saturation as Luminance Varies.
- DP Distortion Appears as Variations in Hue as Luminance Varies.

WHY DOES IT OCCUR?

- Changes in the Amplifier Operating Point Affect the Small Signal Gain and Phase Response.

206627

Stairstep for DG/DP Testing

Micro Seconds
NTC-7 Composite Test Signal
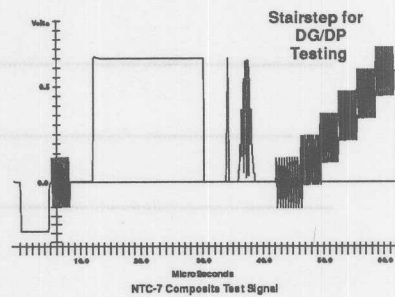
Why are Harris Op Amps
Good Video Performers?

- HARRIS DESIGN TECHNIQUES MINIMIZE DG AND DP ERRORS

  - Outputs are Biased at Higher Currents to Minimize R_O Variations.

  - Series Output Resistors Included to Swamp Transistor R_O.

  - Transistors in AC Path Designed to Tolerate 1V Change in Operating Point.

  - Stacked (Cascode) Current Sources used to Bias AC Path Transistors.

  - Single Gain Stage Design Provides Fewer Error Sources.

206628

Television transmission systems encode the color information through phase and amplitude modulation of the chrominance subcarrier. Thus any subcarrier amplitude or phase distortion introduced during processing or transmission results in imprecise color reproduction. One cause of this distortion is changes in the luminance (brightness) level of the video signal. The luminance level is indicated by the amplitude of the low frequency signal upon which the chrominance signal rides. The amplitude can vary from 0 - 714mV, and sets an amplifier's DC output level. The amplifier's small signal response is a function of the DC level, so distortion of the chrominance signal occurs as the luminance level varies.

Harris op amps are designed to deliver good video performance. Proven methods for minimizing Differential Gain and Phase errors are incorporated into each video amplifier design. The amplifier DC output level is the major factor that sets the output current. Typical Video termination schemes (75-150Ω) dictate large output current variations (0-10mA) as the luminance level changes between it's min and max values. The output current sets the output resistance, which is the main contributor to differential gain and phase errors due to interactions with R_L and C_L.
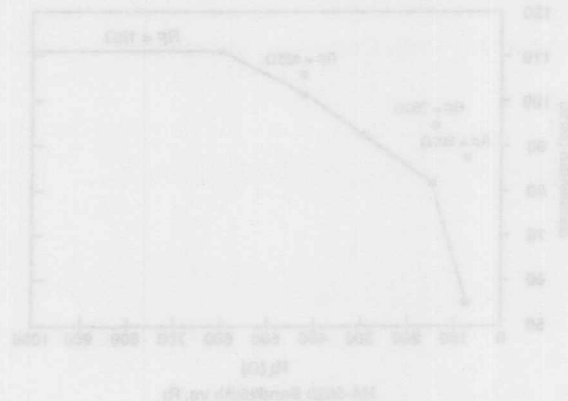
⚏ Performance of Harris Video Op Amps

DEVICE	DESCRIPTION	Diff Gain(%)	Diff Phase(°)
HA-2444	4-Channel; Multiplexed Output; $A_v \geq 1$	0.03	0.03
HA-2544	$A_v \geq 1$; 25mA Output Drive	0.03	0.03
HA-2841	$A_v \geq 1$; Low I_{cc}	0.03	0.03
HA-2842	$A_v \geq 2$; 100mA Output Drive	0.02	0.03
HA-5004	$A_v \geq 1$; 100MHz, Current Feedback	0.04	0.15
HA-5020	$A_v \geq 1$; 100MHz, Current Feedback, Low I_{cc} Output Enable / Disable	0.02	0.03
HA-5033	Unity Gain Buffer, High Output Slew / Drive	<0.1	<0.1
HFA1100/20/30	$A_v \geq 1$, Current Feedback, 850MHz	0.03	0.05
HFA1110/12	Current Feedback Buffers, 850MHz	0.03	0.05

206629

⚏ Current Feedback Amplifiers as Cable Drivers

- **• ONE CFB AMPLIFIER TYPE CAN REPLACE MULTIPLE VFB AMPLIFIER TYPES BECAUSE:**
  - **- BW Virtually Identical at Av = +1 or +2**
  - **- Decreasing R_F Compensates for BW Loss at Low R_L**
  - **- User can Tailor Amplifier to System Conditions via R_F Changes**
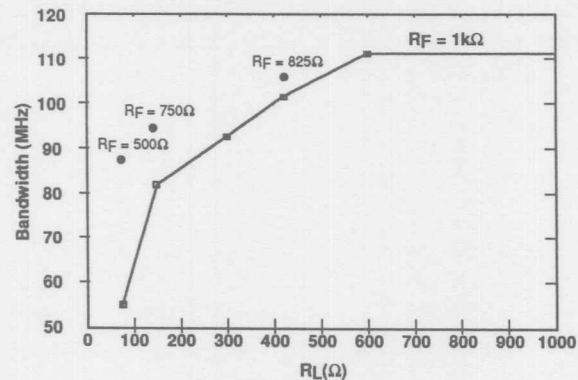
206630   HA-5020 Bandwidth vs. R_L

Harris offers a broad range of amplifiers to meet the varying needs of video designers. From the routine cable driver (HA-2842) to the innovative Video Switching Amplifier (HA-2444), Harris Video Amplifiers are ready to meet the challenge. The HFA11XX family is unique in that it has good DG/DP specs for composite video applications and the excellent gain flatness (to 100MHz) required by component video and HDTV.
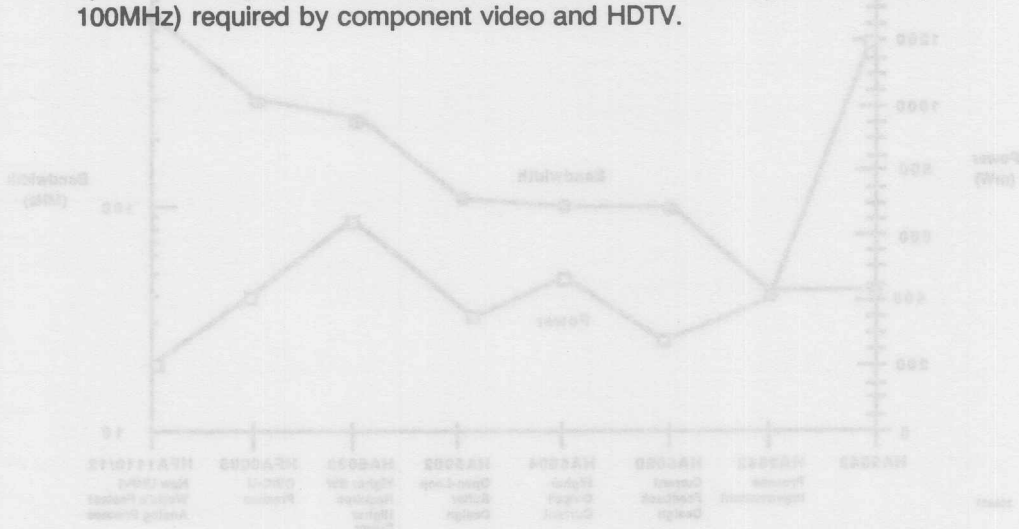
The versatility of CFB amplifiers makes them ideal choices for cable driver applications. Their insensitivity to closed loop gain allows the use of the same amplifier in the signal path, and as the cable driver. Additionally, decreasing R_F compensates for the bandwidth loss at low R_L that is typical of many amplifiers.

The bandwidth versus R_L performance of the HA-5020, with its standard 1kΩ R_F, is depicted by the solid line on the graph. The bandwidth rolloff is quite severe at typical cable driver loads. The three additional points on the graph indicate the increase in bandwidth obtained by choosing a more optimum value of R_F for that specific R_L condition.
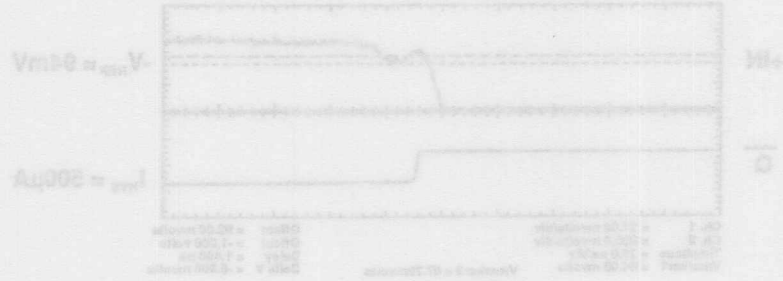
How Can Bandwidth vs. Power Be Improved for Cable Drivers?

Power (mW) / Bandwidth (MHz) chart

	HA2542	HA2842 Process Improvement	HA5020 Current Feedback Design	HA5004 Higher Output Current	HA5002 Open-Loop Buffer Design	HA5033 Higher BW Requires Higher Power	HFA0005 CBIC-U Process	HFA1110/12 New UHF-1 World's Fastest Analog Process

206631
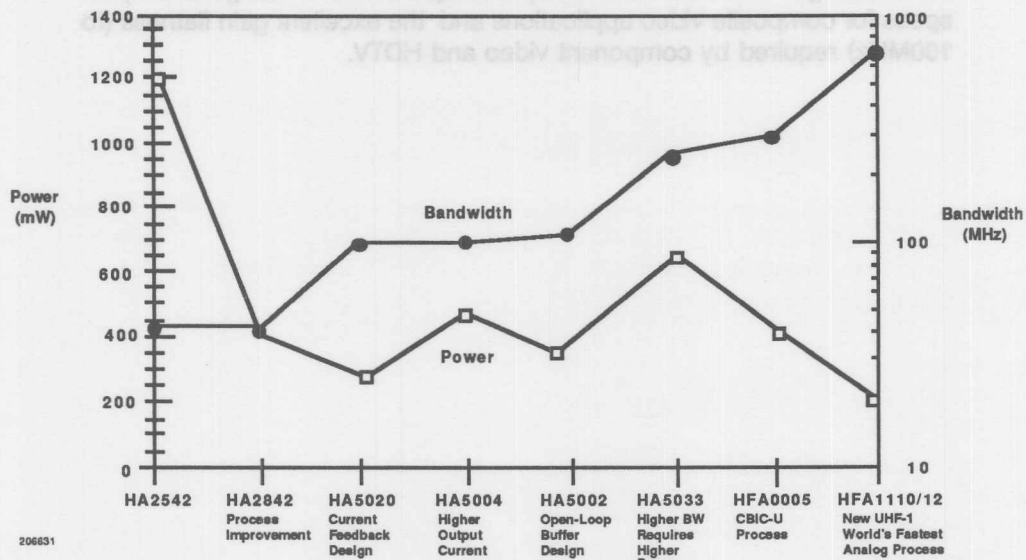
Hysteresis Helps Overcome System Noise Problems

+IN   -V$_{REF}$ = 94mV

Q̄   I$_{HYS}$ = 0

Ch. 1	= 21.00 mvolts/div		Offset	= 92.00 mvolts
Ch. 2	= 600.0 mvolts/div		Offset	= -1.200 volts
Timebase	= 20.0 ns/div		Delay	= 1.400 ns
Vmarker1	= 94.06 mvolts	Vmarker2 = 87.78mvolts	Delta V	= -6.300 mvolts

+IN   -V$_{REF}$ = 94mV

Q̄   I$_{HYS}$ = 500μA

206618

Ch. 1	= 21.00 mvolts/div		Offset	= 92.00 mvolts
Ch. 2	= 800.0 mvolts/div		Offset	= -1.200 volts
Timebase	= 20.0 ns/div		Delay	= 1.400 ns
Vmarker1	= 94.06 mvolts	Vmarker2 = 87.78mvolts	Delta V	= -6.300 mvolts

Improving the speed of high speed cable drivers without increasing the power consumption requires both process improvements and design techniques. This chart shows progressively faster buffers and op amps that are commonly used as cable drivers (and their associated power consumption). Process improvements in the last two years have resulted in two major advances:

1. For ±15V supply operation, a 65% power savings can be seen with the HA2842 (relative to the HA2542).

2. For ±5V supplies, Harris' new UHF-1 process has provided a 150% increase in bandwidth PLUS a 50% reduction in power consumption over the last generation ATT technology.
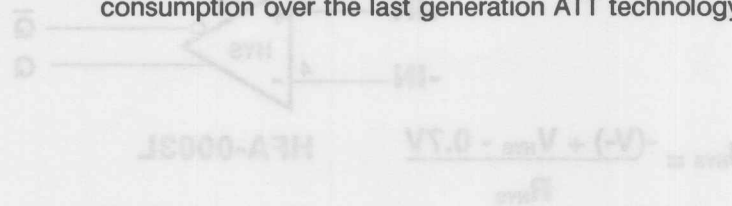
System noise is a major problem when designing with high speed comparators. Input hysteresis helps overcome noise problems by modifying the input switching point each time the comparator detects an input transition through the switching point. This is usually accomplished by building positive feedback into the system. Unfortunately, positive feedback requires numerous external components. The HFA-0003L includes a user programmable hysteresis function. Up to 20mV of input hysteresis may be programmed by setting the current flowing into the HYS pin. The HFA-0003L's built in hysteresis can be activated with a single external resistor to GND.
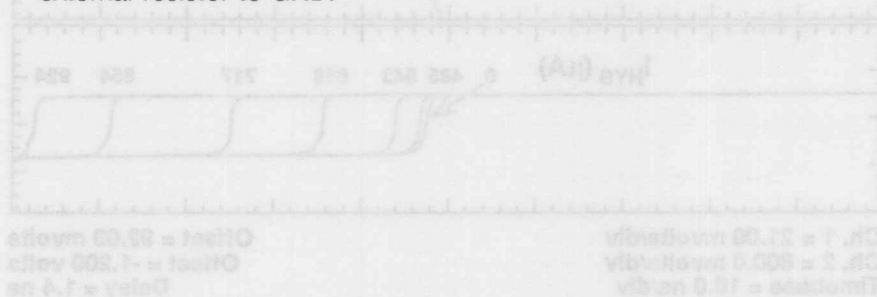
Programmable Hysteresis Under Digital Control

DIGITAL CONTROL SIGNALS

$$I_{HYS} = \frac{-(V-) + V_{HYS} - 0.7V}{R_{HYS}}$$
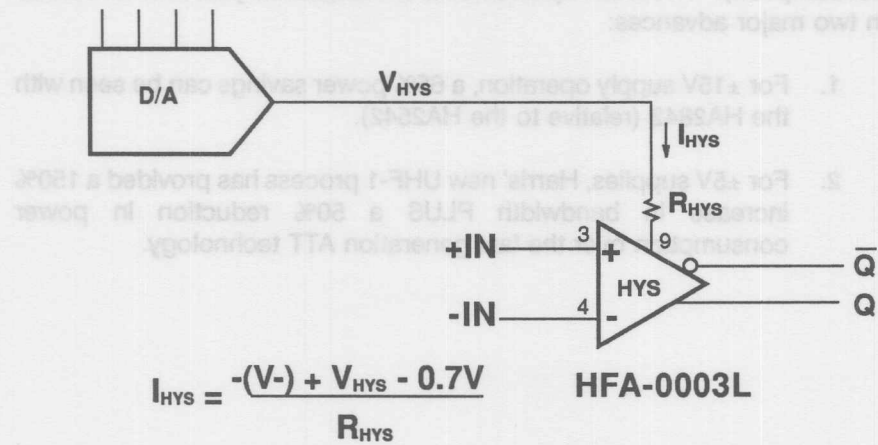
HFA-0003L

206619

HFA 0003L Propagation Delay vs. I_{HYS}

-48.600 ns   1.4 ns   51.400 ns

+IN

V_{OD} = 50mV

$\overline{Q}$

I_{HYS} (μA)   0   485 543   618   717   854   924

Ch. 1 = 21.00 mvolts/div
Ch. 2 = 800.0 mvolts/div
Timebase = 10.0 ns/div

Offset = 92.00 mvolts
Offset = -1.200 volts
Delay = 1.4 ns
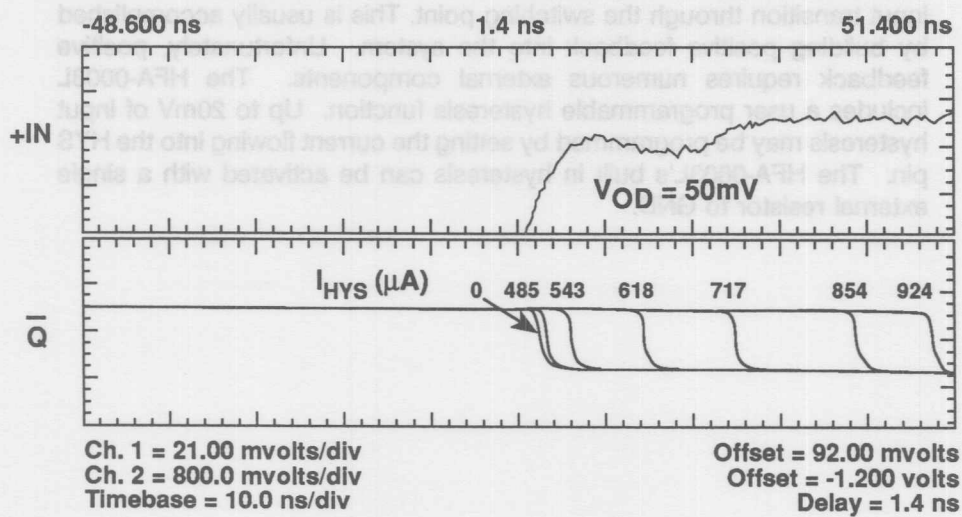
206620

For circuits that would benefit from a variable hysteresis feature (e.g. automatic testers) a D/A can be used to set the current into the HYS input. A digital control word sets the hysteresis voltage, V_{HYS}, which in conjunction with a fixed R_{HYS} determines the hysteresis current. The equation for determining the I_{HYS} is shown below the schematic.
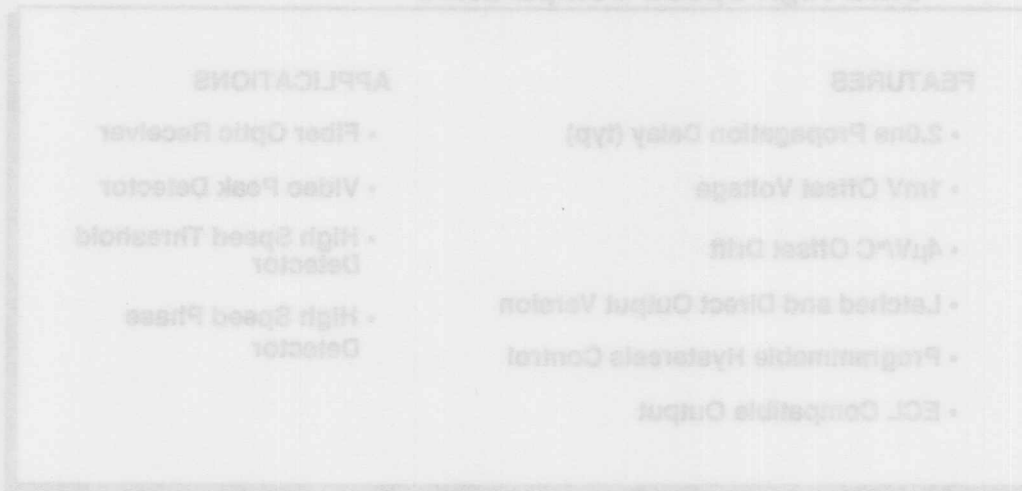
The HFA-0003L propagation delay is a function of the level of hysteresis current. For I_{HYS} = 500µA, the propagation delay is only 600ps longer than the zero hysteresis delay. However, at higher hysteresis currents the impact is more dramatic. Output rise and fall times also begin degrading at hysteresis currents above 500µA, if the input overdrive is small. For the best high speed performance, keep $I_{HYS} \leq$ 500µA.

HARRIS
S E M I C O N D U C T O R
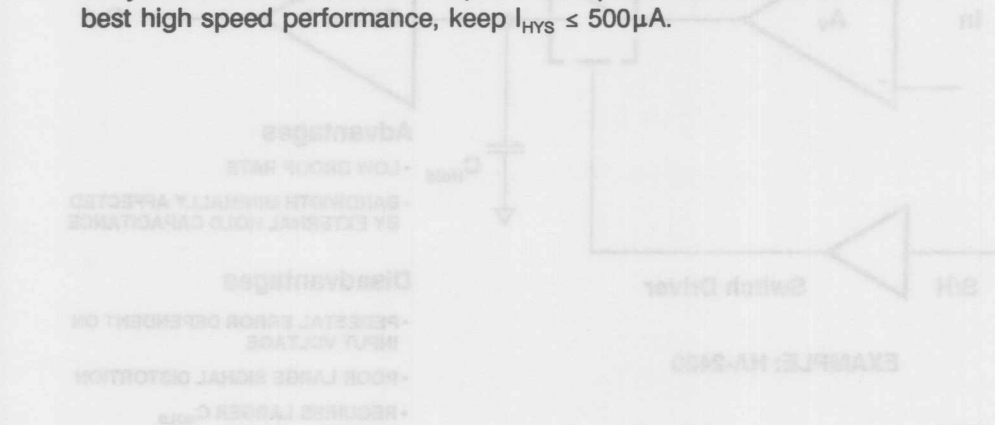
Comparator

HFA-0003 / 3L
Ultra-High Speed Comparators

FEATURES

- 2.0ns Propagation Delay (typ)
- 1mV Offset Voltage
- 4µV/°C Offset Drift
- Latched and Direct Output Version
- Programmable Hysteresis Control
- ECL Compatible Output

APPLICATIONS

- Fiber Optic Receiver
- Video Peak Detector
- High Speed Threshold Detector
- High Speed Phase Detector

206621

Voltage Follower Sample and Hold
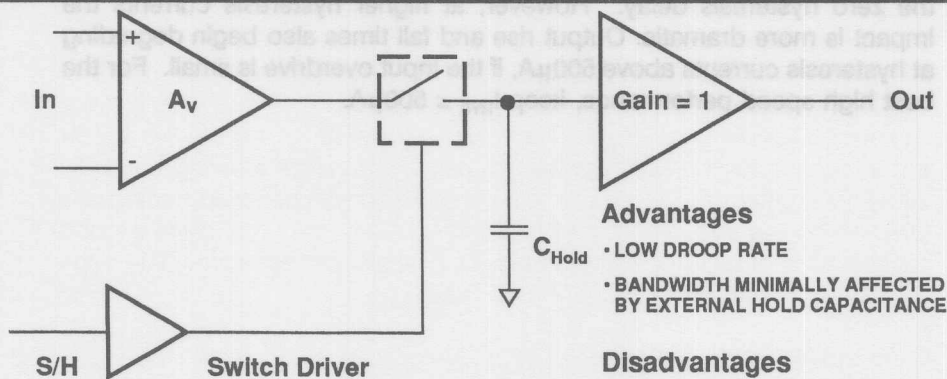
Advantages
- LOW DROOP RATE
- BANDWIDTH MINIMALLY AFFECTED BY EXTERNAL HOLD CAPACITANCE

Disadvantages
- PEDESTAL ERROR DEPENDENT ON INPUT VOLTAGE
- POOR LARGE SIGNAL DISTORTION
- REQUIRES LARGER C_{HOLD}

EXAMPLE: HA-2420

206622

The HFA-0003/3L are monolithic voltage comparators which combine a low V_{IO} with a fast propagation delay. The comparators have differential analog inputs and provide complementary, ECL compatible outputs. The HFA-0003 is a direct output version where the HFA-0003L features a latched output. The latch function allows the comparator to operate in sample-hold or track-hold modes for applications requiring synchronous detection. The HFA-0003L also features the programmable hysteresis function described previously. This feature is not available on the HFA-0003 or on any competitor device.

The HFA-0003 is pin compatible with the MAX9690 and SP9680. The HFA-0003L is pin compatible with the MAX9685, AD96685 and SP9685.

It is important to maximize the signal swing prior to the analog to digital converter to maximize ADC resolution. Unfortunately, this requires the sample and hold to operate under large signal conditions. Therefore, large signal distortion is of primary concern.

The first architecture developed to solve this problem was the Voltage Follower Sample and Hold. The hold capacitor is driven by a low impedance voltage gain input stage, capable of large slewing currents, allowing large amplitude signals to be processed with bandwidth minimally affected by the size of the hold capacitor. Within limits this gives a good combination of fast acquistion time with a large hold capacitor. The large capacitor making possible low droop rate.

A drawback of this architecture is the exposure of the switch to the signal voltage. As the signal voltage changes, the charge on the parasitic capacitances of the switch devices will also change. When the switch is "opened" a portion of this charge will be injected onto the hold capacitor, producing a voltage step error or "pedestal error". This variation in pedestal error cannot be calibrated out and therefore contributes to distortion. On the HA-2420 with a 1000pf hold capacitor, the pedestal will vary about 8mV for input swings from -10V to +10V.

Integrating Sample and Hold

In → Gm (+/−)

C_{Hold}

− A_V + → Out

Z_s

S/H → Switch Drive

Advantages
- PEDESTAL ERROR INDEPENDENT OF INPUT VOLTAGE
- FAST ACQUISITION TIME
- HIGH SLEW RATE WITH SLEW ENHANCEMENT CIRCUIT

Disadvantages
- POOR LARGE SIGNAL DISTORTION (DUE TO SLEW RATE ENHANCEMENT)
- INCREASED C_{HOLD} WILL DIRECTLY AFFECT BANDWIDTH
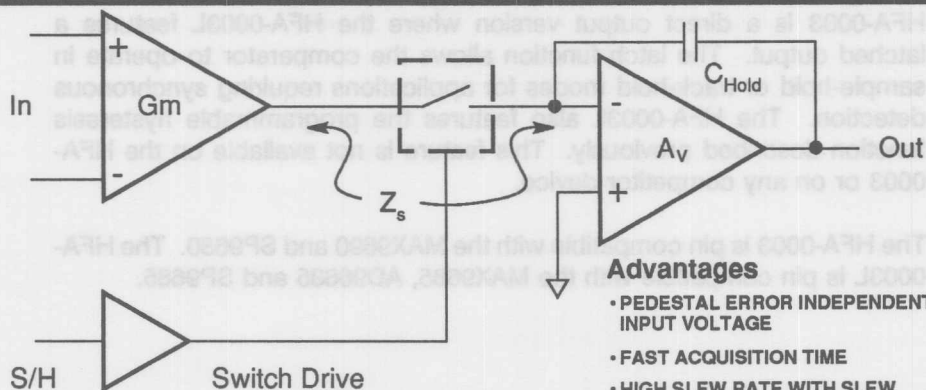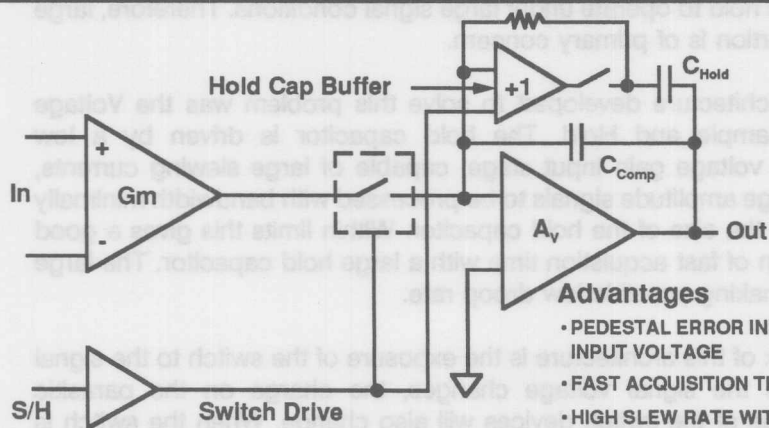
EXAMPLE: HA-5320
HA-5330

206623

Improved Integrating Sample and Hold

Hold Cap Buffer → +1

C_{Hold}

In → Gm (+/−)

C_{Comp}

A_V → Out

S/H → Switch Drive

Advantages
- PEDESTAL ERROR INDEPENDENT OF INPUT VOLTAGE
- FAST ACQUISITION TIME
- HIGH SLEW RATE WITHOUT ENHANCEMENT CIRCUIT
- BANDWIDTH MINIMALLY AFFECTED BY EXTERNAL HOLD CAPACITOR
- LOW LARGE SIGNAL DISTORTION

EXAMPLE: HA-5340

206624

This architecture uses a transconductance input stage to force charge into a virtual ground until an integrating hold capacitor is charged with the desired voltage. The problem of the voltage dependant pedestal goes away because both sides of the switch are always at virtual ground.

The integrating sample and hold typically has a very large open loop gain, because the overall amplifier is a cascade of two amplifiers. The large gain insures excellent signal linearity which makes it a good choice in systems that require 12 bits of precision or beyond.

However, there are some drawbacks also. The Acquisition Time is directly affected by the size of the hold capacitor. During acquisition the input Gm stage develops its maximum output current to charge the hold capacitor, no matter what size it may be. The Output Slew Rate becomes limited by I(Gm)/C(hold). Also, the hold capacitor acts as the compensation and without slew enhancement circuits these amplifiers would be very slow for the same supply current as a voltage follower type.

The patented architecture of the Improved Integrating Sample and Hold used in the HA-5340 takes the advantages from both previous designs. First, the voltage dependant pedestal is avoided with an integrating structure and the Slew Rate limitation on the Hold Capacitor is avoided with the addition of a voltage output buffer. This buffer can provide the current necessary to charge the hold capacitor without limiting the Slew Rate or Bandwidth. In hold mode the Hold Cap Buffer goes to a high impedance state, allowing a resistor to provide output stage feedback.

This new architecture gives the speed advantages of the Voltage Follower with the reduced pedestal distortion of the virtual ground switch. There is no longer a need for a Slew Enhancement circuit and therefore the part can be optimized for low distortion.

⊞ THD in Hold Mode vs Sample Mode For the HA-5340 and HA-5320

THD vs. Frequency

THD values on Y-axis: -20dBc, -40dBc, -60dBc, -80dBc, -100dBc

HA-5320
Sample and Hold Modes

HA-5340
Hold Mode

HA-5340
Sample Mode

Frequency (Hz) V$_{out}$ = 5V$_{pp}$

0   100k   200k   300k   400k   500k

f$_{sample}$ ≈ 450kHz

THD vs. V$_{OUT}$

THD values on Y-axis: -20dBc, -40dBc, -60dBc, -80dBc, -100dBc

HA-5320
Sample and Hold Modes

HA-5340
Hold Mode

HA-5340
Sample Mode

V$_{out}$ (p-p) @200kHz

5   10   20

f$_{sample}$ ≈ 450kHz
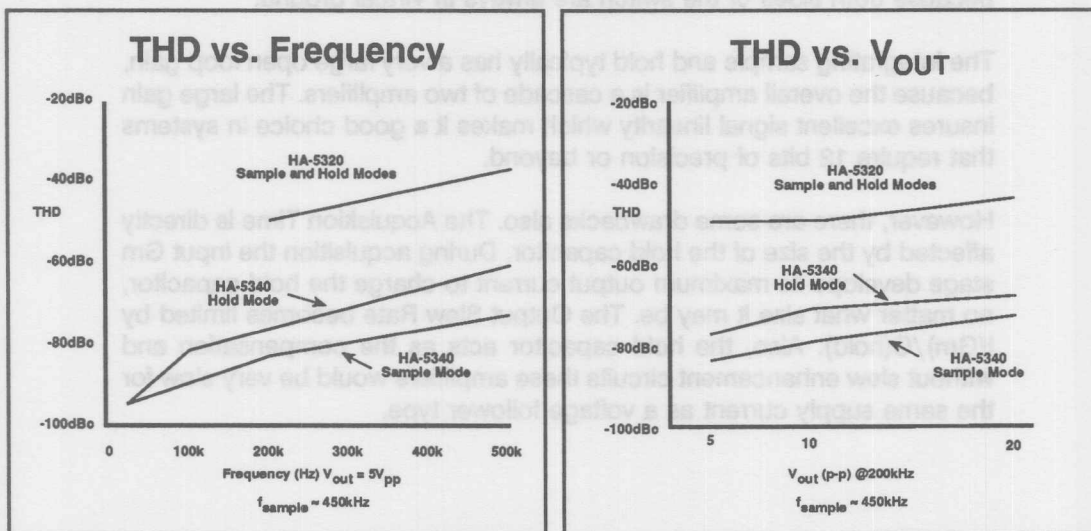
206625

⊞ Sample Mode Harmonic Distortion

HA5330

HA5320

HA5340

GENERATOR

THD (dBc): -30, -40, -50, -60, -70, -80, -90

INPUT VOLTAGE (V$_{P-P}$): 0.01   0.1   1   10
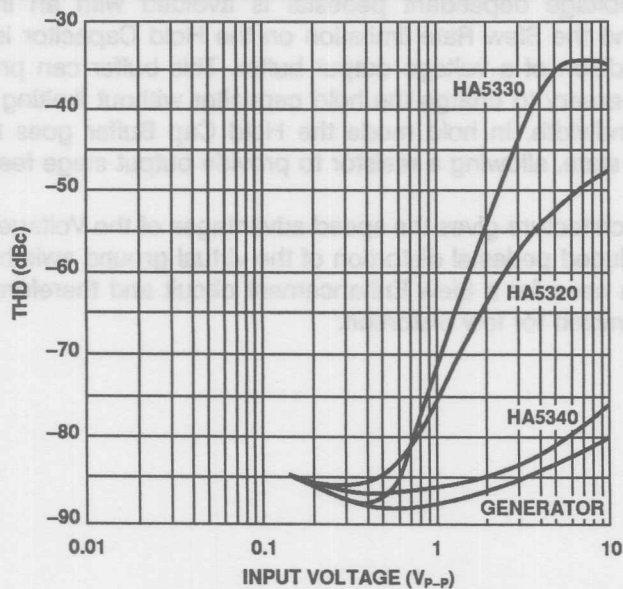
206626

The graphs show a comparison of Total Harmonic Distortion for the Integrating type Sample and Hold, the HA-5320, and the Improved Integrating Sample and Hold, the HA-5340. The graph also indicates two types of distortion; Sample Mode and Hold Mode.

THD specifications may refer to sample mode or hold mode. For high speed data acquisition systems, where the Sample and Hold captures data for conversion by an ADC, the amplifier distortion is largely irrelevant. Hold Mode distortion contains additional error contributions from hold mode settling time, droop rate, hold mode feedthrough, as well as a change in the output impedance when the part goes into Hold Mode.

For example, the HA-5340 shows that at a 200KHz, 5Vp-p input signal, the amplifier or Sample Mode total harmonic distortion is -83.56dBc. However when the device is operated at a 450KHz sample rate and only held data is evaluated, the distortion increases to -76.95dBc.

In contrast, the HA-5320 standard integrating Sample and Hold, has a Sample Mode distortion of -49.7dBc. Here the slew rate enhancement distortion dominates so the Hold Mode THD does not significantly increase.

Distortion occurs when devices do not operate in their linear regions. This can occur in sample-and-hold amplifiers if they are required to deal with large signal levels. This chart shows the Total Harmonic Distortion vs. peak-to-peak input voltage performance of several sample-and-hold devices. The input signal frequency is 200KHz. In order to minimize distortion, the HA5340 has a specially designed input stage that does not go into overload for large voltage swings. In contrast, the HA5330 has slew enhancement circuitry which enables it to have faster acquisition time than the HA5340 but also causes distortion.

UHF-1 High Speed Analog Process

Features

- 8GHz NPN, 4GHz PNP
- DOUBLE LEVEL METAL TECHNOLOGY
- 10 x IMPROVEMENT IN AC PERFORMANCE
- MINIMUM EMITTER IS 3 MICRON BY 4 MICRON
- HIGH SPEED AT LOWER POWER

- BONDED WAFER DI
- COMPLEMENTARY BIPOLAR
- SELF-ALIGNED POLY-EMITTER
- JFET
- TRIMMABLE THIN FILM RESISTOR

206632

UHF-1 Cross Section

Comparison of UHF-1 with Prior Generation DI Process Showing Size Reduction
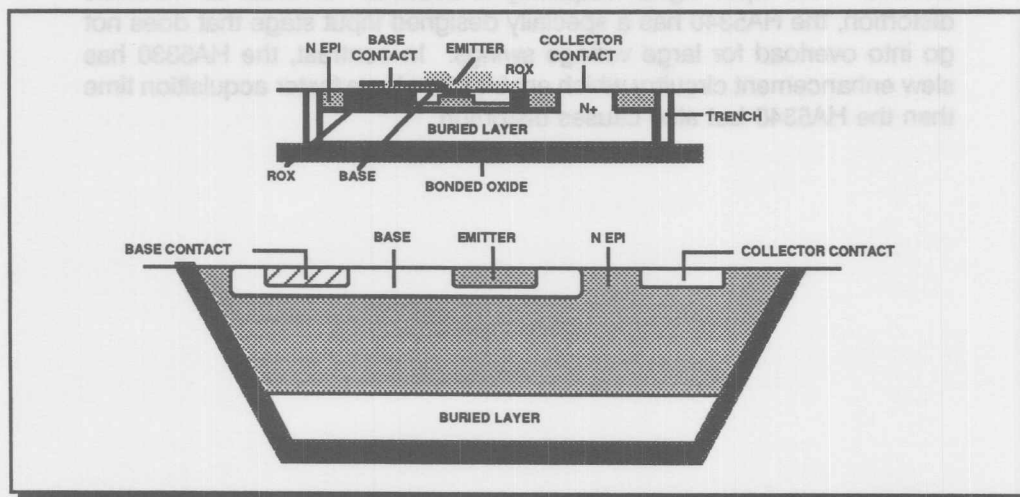
206633

UHF-1 is an ultra-high frequency complementary bipolar process. Digital ECL (Emitter Coupled Logic) processes that are optimized for fast switching have achieved higher NPN speeds, but they lack the PNPs needed for analog circuits. Fast PNPs and NPNs in the same process allow analog IC designers to achieve higher speed at low power and simplified circuit designs. The bonded wafer DI (Dielectric Isolation) process pioneered by Harris also simplifies the circuit design, because each transistor is fully isolated from other transistors and the substrate.

The UHF-1 process owes much of its speed to the much smaller transistor size, compared with previous complementary processes. The smaller transistor size is also what limits the supply voltages to +5V instead of +15V for the previous processes.

The UHF-1 transistor speed is also increased by minimizing "stray" capacitances. The use of "trench" etching creates isolation walls around the transistors that are more vertical (with lower capacitance) than in previous processes. The Rox implant between the collector and the emitter in UHF-1 also lowers the capacitance of the transistors.

How are Bonded Wafers Made?

(a)
Wafer 1

Thermal Oxide

Wafer 2

(b)
Wafer 1

Bonded Oxide (isolation)

Wafer 2

(c)
Oxide

Wafer 2 (handle)

(d)
n-epitaxial layer

n+ buried layer (thinned wafer 1 after diffusion)

Oxide

Wafer 2 (handle)

(e)
Oxide   Polysilicon   Isolated Island   Trench   Epitaxial silicon

n+ buried layer

Oxide

Wafer 2 (handle)
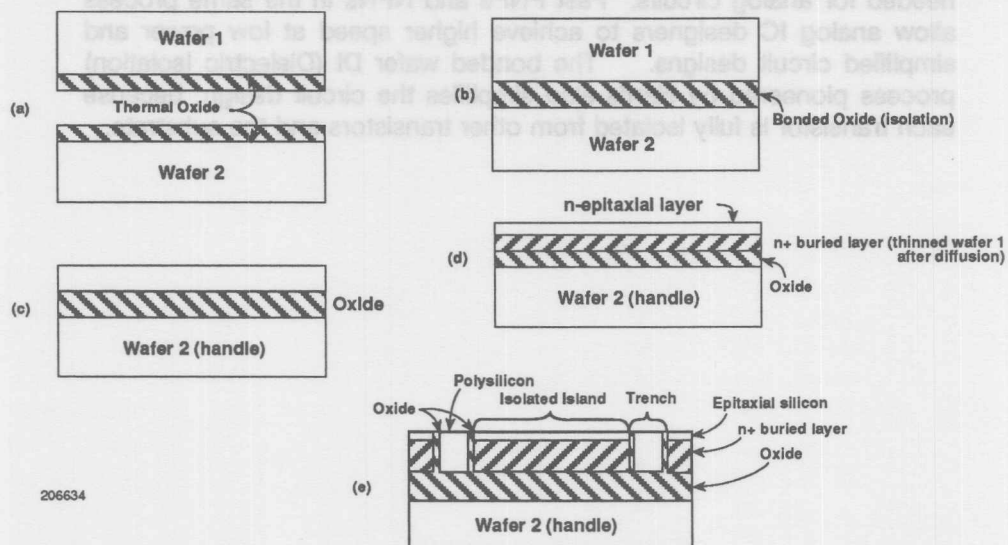
206634

Flagship Products on UHF-1

- **HFA11X0**   **850MHz Current Feedback Op Amps**

- **HFA1110/12**   **850MHz Closed-Loop Buffers**

- **HFA11X5**   **400MHz, 50mW Op Amps**

- **HFA3XXX**   **Transistor Array Family**

- **HFA5250**   **Pin Driver for A.T.E.**

206635

Wafer bonding is required to make the high performance UHF-1 process. Harris is the first company in the industry to commercialize this type of process.

(a) Thermal oxide layers are grown on two silicon wafers.

(b) These wafers are then bonded together.

(c) One wafer is then used as the "handle" as the other is ground down until the silicon is very thin.

(d) A buried layer (critical for high speed transistors) is then made in the thinned-down silicon. Then an n-epi layer is grown. The collector, base and emitter of each transistor are eventually implanted into the epi layer.

(e) The transistors are isolated from each other by "digging" trenches (down to the original oxide) around the transistor "islands". The sides of the trenches are coated with oxide and then refilled with polysilicon in order to make them mechanically strong.

A variety of standard analog building blocks are now offered from Harris built on the UHF-1 process. These include the world's fastest op amps, buffers with excellent speed/power performance and transistor arrays that include combinations of NPNs and PNPs as individual transistors or connected as differential inputs. Also available is a 500MHz pin driver that is designed into high speed digital IC test equipment.

HARRIS
SEMICONDUCTOR

UHF-1 ASIC Capabilities

**Customer Access
to UHF-1 for:**

**FASTRACK Design System
Tile Array
and
Device Level Design**

• RADAR SIGNAL PROCESSING	• MIXED SIGNAL APPLICATIONS	• VIDEO SIGNAL PROCESSING CHAINS	• COMMUNICATIONS
- Prescalers - RF Signal Conditioning	- High Speed, High Accuracy - Low-Power ECL Replacement	- Broad Bandwidth - Fiber Optic Interface - High Resolution Video Displays	- Cellular Telephone - Telemetry
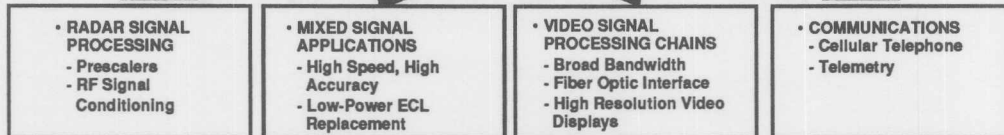
206636

You can also use the performance of UHF-1 when doing semicustom analog design. UHF-1 based circuits are available in both tile arrays, ASICs and full-custom, device level design. Customers with applications in Radar, Instrumentation, Video Signal Processing and Communications (and other high speed analog applications) will be able to develop dedicated circuits on the world's fastest complementary bipolar process. Harris' award winning FASTRACK design system greatly increases the likelihood of first pass success.

Harris Semiconductor

COMMUNICATIONS

IMAGING

ATE

SIGNAL GAIN

X

SIGNAL
CONDITIONING

$f(t)$

ADC DRIVER

ANALOG to DIGITAL

00110

DSP

DIGITAL to ANALOG

00110

SIGNAL
CONDITIONING

$f(t)$

MULTIPLEX

CABLE DRIVER

208637
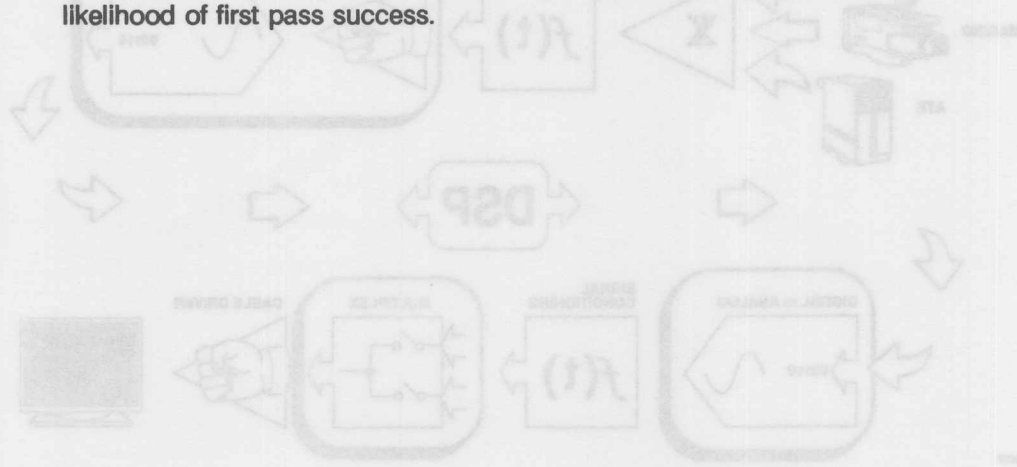
DATA CONVERSION
TECHNIQUES
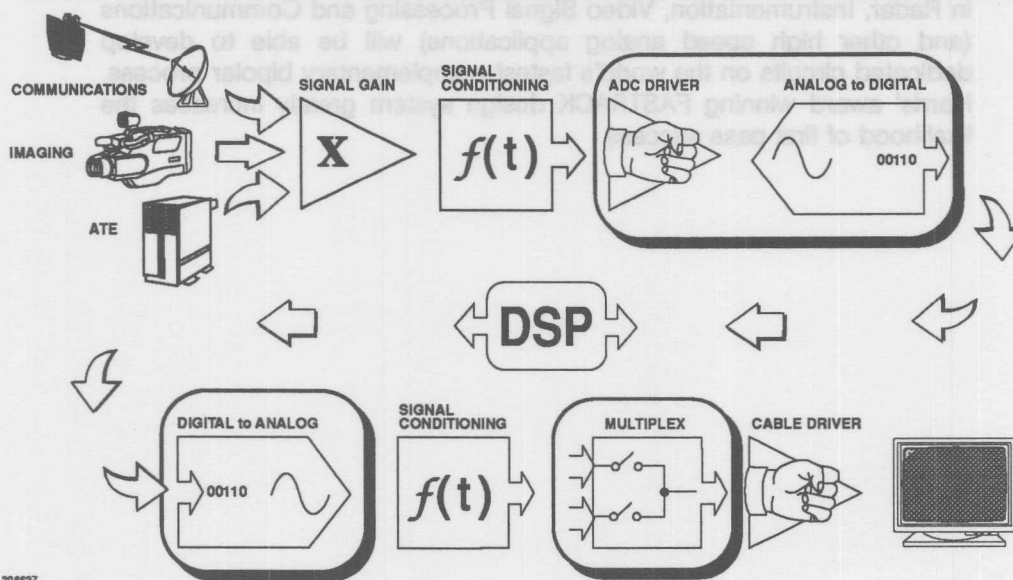
Flash Converter Analog Input Drive Considerations

- ANALOG INPUT RANGE

- INPUT CAPACITANCE

- DYNAMIC PROPERTIES - THD, SNR

206638

Minimum Buffer Requirements
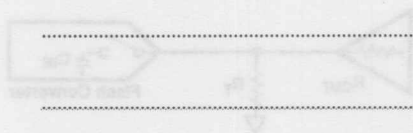
- **Output Swing**
  Unipolar 0V to +4V (Vref+)
- **Power Bandwidth of System (PBW)**
  5MHz Minimum
- **Minimum Slew Rate (SR)**
  $SR_{min} = 4V/0.25$ Pixel Period $= 400V/\mu S$
- **Total Harmonic Distortion (THD)**
  -54dBc @ 5MHz
- **Output Drive Current (I_{out})**
  $I_{out}min = C_{in}(dv/dt) + I_{term} + I_{FB}$
  $= 24mA + 40mA + 0 = 64mA$
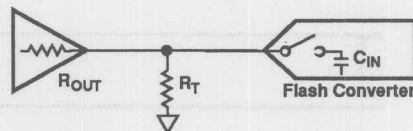
206639

The analog input to the HI-5700 flash A/D converter is unipolar (0V to Vref+). The analog signal source or reference inputs must not exceed the power supply rails (VDD or GND) by more than 0.5V to prevent device degradation or latchup.

In general, the input to a flash A/D needs to be amplified or buffered for the following reasons:

1) to adjust gain and offset
2) to sink any spurious clock kick back generated during the conversion process
3) to drive the A/D's input capacitance.

In the video demo, both full scale and offset adjustments are performed with the HA-2546 video multiplier.

An amplifier or buffer must be selected which will not degrade the performance of the A/D. The primary consideration is to match the dynamic performance of the buffer to the flash converter. The amplifier must exhibit low harmonic distortion, wide bandwidth, high slew rate, fast settling, and low output impedance at the frequency of interest.

The input to the HI-5700 should be driven by a high output drive amplifier or buffer. Although the HA-5020 can directly drive the HI-5700, the HA-5033 has better current drive, lower output impedance and higher bandwidth.

CURRENT DRIVE - It is important that the transient spike (caused by the switching of the internal CMOS comparators) is dissipated to ensure conversion accuracy. The minimum amplifier output drive current is a function of the maximum slew rate, termination load resistance and feedback current, if any.

HIGHER BANDWIDTH - The demo system must digitize video signals having approximately 5MHz bandwidth. The amplifier bandwidth must be greater than that of the converter. Insufficient amplifier bandwidth introduces distortion because of phase nonlinearity due to high frequency rolloff.

The minimum slew rate that is required for a 4V swing in one quarter of a pixel period is 400V/µs. An amplifier with a greater slew rate than is actually needed should be selected. When an amplifier approaches slew rate limiting it becomes nonlinear causing settling problems (distortion).

Wideband Amplifier Combines System Gain and ADC Driver

BEST!

402Ω
48Ω
1KΩ
HFA1100
100Ω
C
V_IN
ADCLK
CLK
HI-5700

ADCLK

BETTER

402Ω
48Ω
402Ω
HA-5020
+1
HA-5033
100Ω
B
V_IN
ADCLK
CLK
HI-5700
1KΩ

C

B

A

NOPE!

402Ω
48Ω
1KΩ
HA-5020
100Ω
A
V_IN
ADCLK
CLK
HI-5700
FLASH A/D
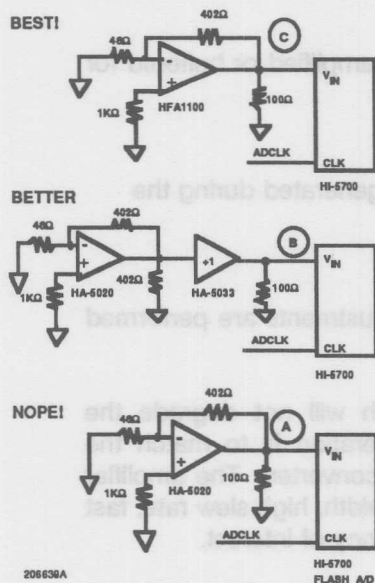
206639A
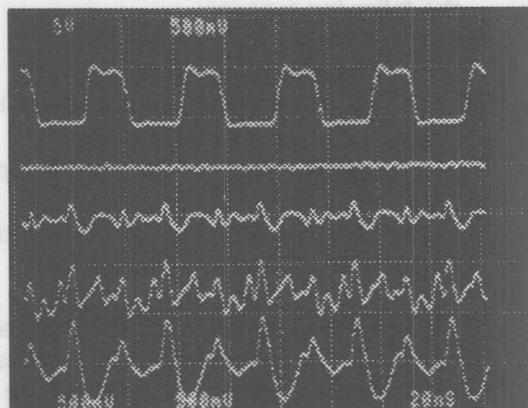
Reference Requirements

REF101
V_out
Feedback
R_A
V_CC
GND
R_B
+4V
+15
0.1
0.001
10
38.3K
R_2
R_11
1.47K

HA-5177
HA-5002
10
10
0.1
0.001µF
To A/D Converter

V_REF
To 2 D/A Converters

- **+4V STABLE VOLTAGE REFERENCE**
- **117mA CURRENT CAPABILITY**

206640

It is often difficult to find an amplifier that can provide system gain while maintaining the low output impedance required for driving an ADC. An output impedance that is too large results in unacceptable output excursions caused by the ADC "kickback". Because op amp output impedance is reduced by it's loop gain, the minimum output impedance is obtained at DC with the lowest closed loop gain. Higher closed loop gains increase the DC impedance while high frequency signals, like kickback, see a much larger impedance due to the decrease in open loop gain.
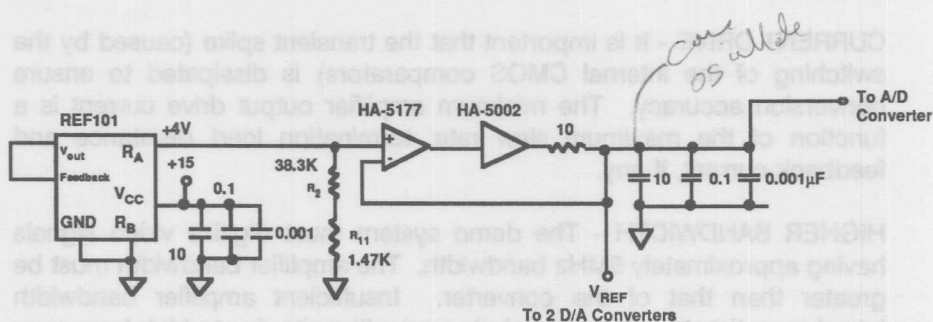
Waveform A shows an attempt at driving the HI-5700 8-bit Flash Converter with a 100MHz Current Feedback Amplifier (CFA). Despite it's low DC output impedance, the HA-5020 in a gain of 10 can't handle the HI-5700 kickback. A solution is to add a buffer to drive the ADC. Waveform B shows the considerable improvement obtained with this approach.

The best results, in terms of complexity and glitch suppression, are obtained by simply using a wideband amplifier as the gain/driver stage. The HFA1100, with it's 850MHz bandwidth, maintains a very low output impedance, even at high closed loop gains with high frequency signals. Waveform C shows the low dynamic output impedance and fast settling characteristic of the HFA1100 driving the HI-5700.

A system voltage reference is constructed using a REF101 in conjuction with a composite amplifier employing the HA-5177 and HA-5002. This combination provides a precision +4V, 2ppm/°C tempco reference having sufficient drive current capability for the HI-5700 and two CA3338s. The REF101 4V output is obtained by modifying the precision internal voltage divider ratio by placing an external resistance between RA and RB terminals. The tempco of the external resistance must ideally match the internal resistor's (50ppm/°C) to not degrade the tempco of the reference. The HA-5177 features an ultra low offset voltage of $25\mu V$ max at 25°C having an offset voltage drift of $0.3\mu V/°C$ max. The HA-5002 has a typical output resistance of 3Ω, provides 200mA current output and is capable of driving large capacitive load without oscillation.

HI-5700 reference voltage terminals are subjected to internal transient currents during conversion. It is important to drive the reference pin from a low impedance source and to decouple thoroughly between $V_{REF(+)}$ and $V_{REF(-)}$ pins. Ceramic and tantalum ($0.01\mu F$, 0.1uF and $10\mu F$) capacitors near the package pin are recommended. Typically,it is not necessary to decouple the 1/4 REF, 1/2REF and 3/4REF tap point pins. Here, a 33pF ceramic capacitor decouples the 1/4REF point for best performance.

Reducing the reference voltage reduces the LSB size proportionately and will increase linearity errors. Minimum practical reference voltage is 2.5V.

Alternate Reference

$$V_{Ref} = (1.2V) \left(1 + \frac{R_2}{R_1}\right)$$
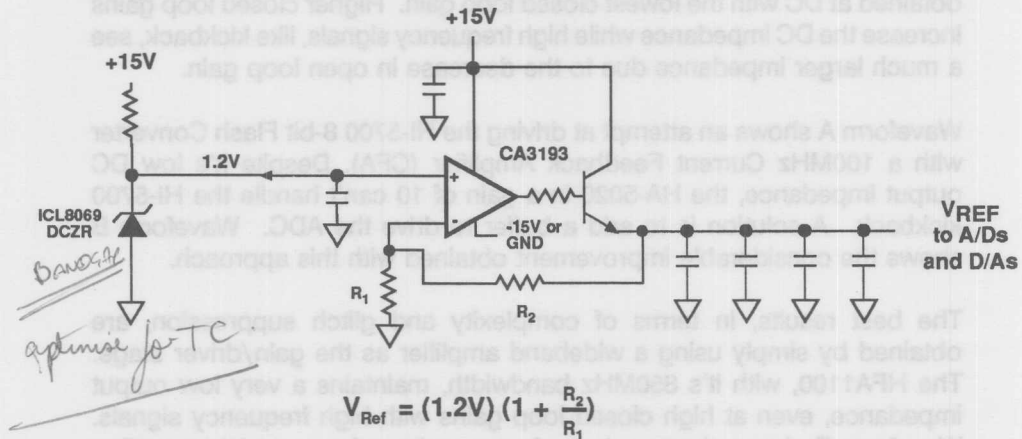
206641

Flash A/D Converters

Simplified Block Diagram
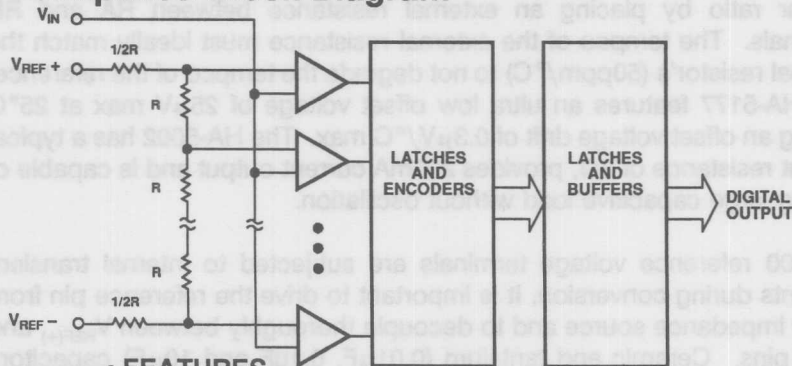
• FEATURES

2^N-1 Comparators (N = Bits)

Conversion in One Clock Cycle

Fastest Type of Converter

206642

This reference circuit is comprised of a voltage reference, amplifier and series pass transistor. It uses a 50ppm/°C 1.2V bandgap voltage reference. A series pass NPN transistor provides the necessary load current. The resistor between the amplifier and base of the NPN transistor helps to prevent oscillation as the circuit can drive large capacitive loads. The reference output voltage is set by the ratio of the feedback network.
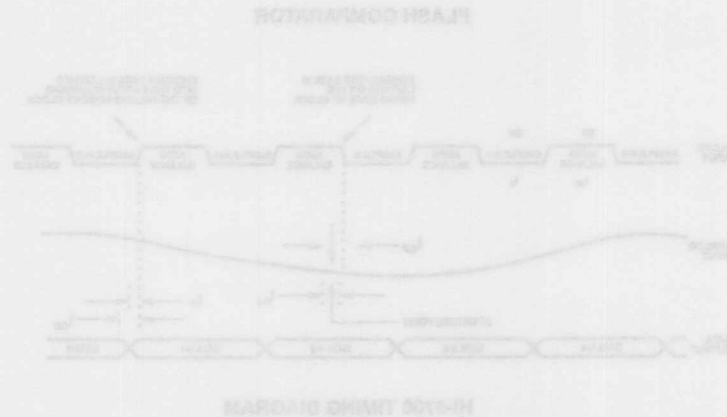
The HI-5700 is an 8-bit analog-to-digital converter based on a parallel "flash" architecture. The HI-5700 uses 255 (2^8-1) comparators to encode the 8 bit data output, plus an additional comparator to detect Overflow. This flash technique is the fastest method of A/D conversion because all bit decisions are made simultaneously.

The analog signal is simultaneously applied to all of the comparator inputs. The other input to each comparator is connected to a tap on the resistor divider network which establishes a reference potential for each comparator in 1 LSB increments. The thermometer code output from the comparator array is latched and is encoded into a binary format. The resulting binary data is then latched and presented to the output buffers.

HI-5700
8-Bit, 20MSPS Flash A/D Converter

V$_{IN}$ ○ ⊗ Ø2 — Ø1 ⊗
TO LATCHES &
ENCODER LOGIC

TO RESISTOR
LADDER TAP ○ ⊗ Ø1

FLASH COMPARATOR

COMPARATOR DATA IS
LATCHED ON THE
RISING EDGE OF CLOCK

ENCODER DATA IS LATCHED
INTO THE OUTPUT REGISTERS
ON THE FALLING EDGE OF CLOCK

CLOCK
INPUT | SAMPLE N-2 | AUTO BALANCE | SAMPLE N-1 | AUTO BALANCE | SAMPLE N | AUTO BALANCE | SAMPLE N+1 | AUTO BALANCE | SAMPLE N+2 | AUTO BALANCE

t_{AB} t_S

ANALOG
INPUT

t_{AP} →

← t_{AJ} t_H

APERTURE POINT

← t_{OD}

DATA
OUTPUT | DATA N-4 | DATA N-3 | DATA N-2 | DATA N-1 | DATA N

HI-5700 TIMING DIAGRAM

206644

- **FEATURES**

  - **Single 5V Supply**

  - **20MSPS Conversion Rate**

  - **18MHz Full Power Bandwidth**

  - **CMOS/TTL Compatible**

  - **Improved Replacement for MP7684**

- **APPLICATIONS**

  - **Video Digitizing**

  - **Medical Imaging**

  - **Communication Systems**

  - **High Speed Data Acquisition**

206645

The HI-5700 ADC comparator architecture alternately switches between "Sample" and "Auto-Balance" modes. The offset voltage of each CMOS comparator is dynamically cancelled with each conversion cycle such that offset voltage drift is virtually eliminated during operation.
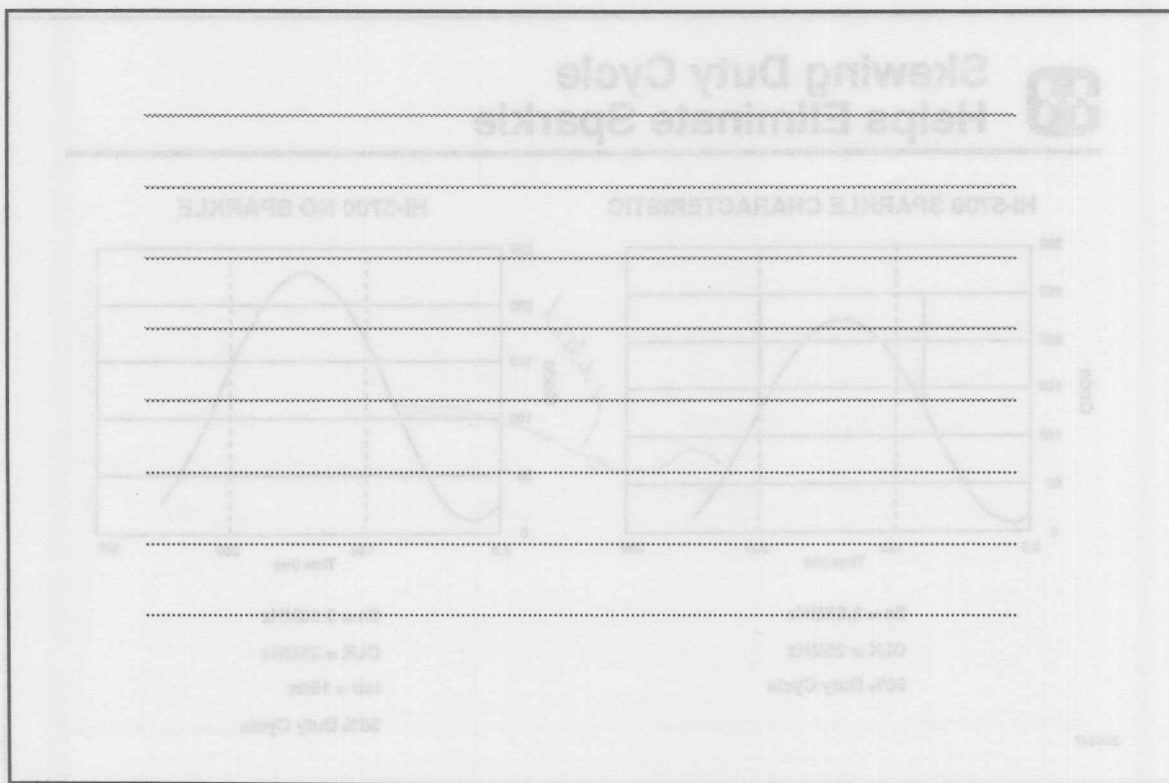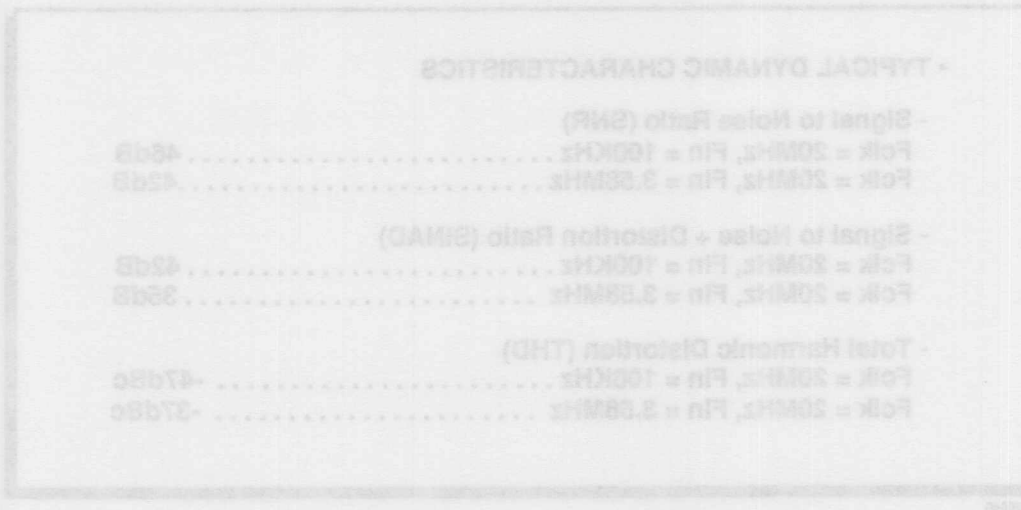
HI-5700
20MSPS Flash A/D Converter

• **TYPICAL DYNAMIC CHARACTERISTICS**

- **Signal to Noise Ratio (SNR)**
  Fclk = 20MHz, Fin = 100KHz 46dB
  Fclk = 20MHz, Fin = 3.58MHz 42dB

- **Signal to Noise + Distortion Ratio (SINAD)**
  Fclk = 20MHz, Fin = 100KHz 42dB
  Fclk = 20MHz, Fin = 3.58MHz 35dB

- **Total Harmonic Distortion (THD)**
  Fclk = 20MHz, Fin = 100KHz . . . . -47dBc
  Fclk = 20MHz, Fin = 3.58MHz . . . . -37dBc

206646

Skewing Duty Cycle
Helps Eliminate Sparkle

HI-5700 SPARKLE CHARACTERISTIC
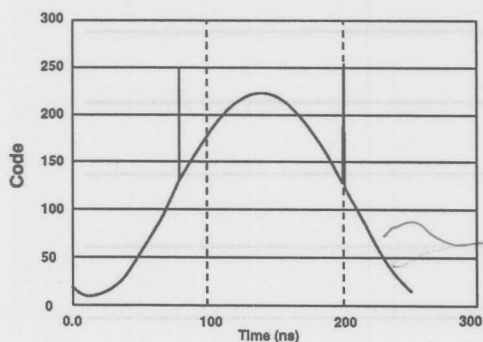
fin = 3.98MHz

CLK = 25MHz

50% Duty Cycle

HI-5700 NO SPARKLE
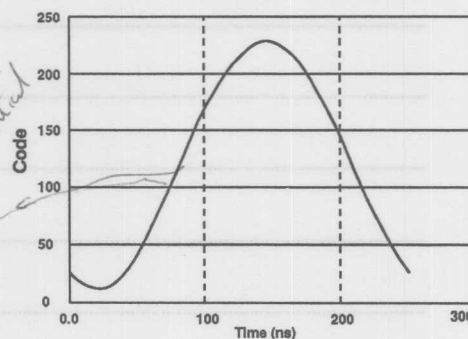
fin = 3.98MHz

CLK = 25MHz

tab = 15ns

38% Duty Cycle

206647

The signal-to-noise ratio (SNR) is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies. For a 100KHz sine wave input and 20MHz sample rate the typical SNR measures 46dB.

The signal-to-noise & distortion (SINAD) is the ratio in dB of the RMS signal to RMS sum of the noise and harmonic distortion at specified input and sampling frequencies. The theroretical limit for an ideal 8 bit converter having no linearity errors is 49.9dB (SINAD = 6.02N + 1.76). For 100KHz and 3.58MHz sine wave inputs and 20MHz sample rate the typical SINAD measures 42dB and 35dB respectively. The 100KHz and 3.58MHz inputs translate to 6.7 and 5.5 effective bits respectively.

Total harmonic distortion (THD) is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specifed input and sampling frequency. For a 100KHz sine wave input & 20MHz sample rate the typical THD measures -47dBc.

System timing requirements mandate that the HI-5700 flash A/D converter operate the HI-5700 with a 25MHz clock although it is specified only at 20MHz clock. The major problem encountered with 25MHz operation is sparkle. By changing the duty cycle of the clock the part has been shown to work reliably at 25MHz or higher at 25°C. The datasheet specifies a 20MHz clock with a 50% duty cycle which gives minimum "sampling" and "auto balance" times of 25ns each. It was determined that 25MHz clock operation is achievable by reducing the minimum "auto balance" time (t_{AB} or ϕ 1) to 15ns and retaining the minimum "sampling" time (t_S or ϕ 2) at 25ns.

A benefit of skewing the duty cycle is a slight reduction in power consumption. In the demo a 10% power reduction is seen for the HI-5700.

HI5700 Evaluation Board

206649
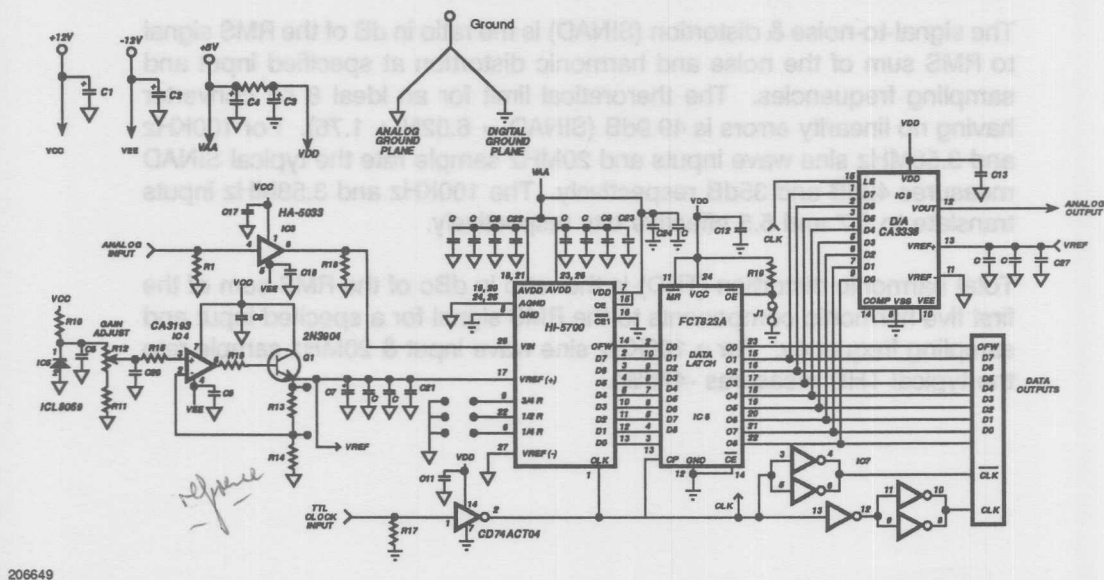
Automatic Gain Control
Multiplying DAC as Stage 2 Variable Gain Resistor
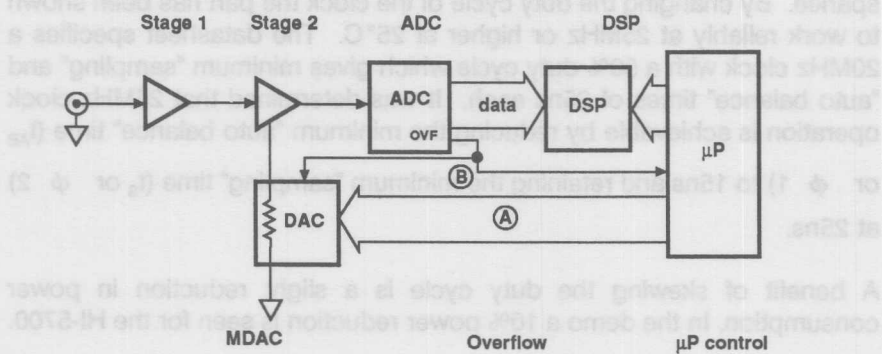
- (A) μP CONTROLS GAIN BY CHANGING DAC RESISTANCE

- (B) ADC OVERFLOW BIT REDUCES GAIN, PROVIDES INPUT TO μP

206650

*Multiplying DAC = variable resistor
But will lose B.W. so use this config.*

58

Layout is one of the most important considerations when designing a high speed data conversion board. Standard RF layout techniques include using ground planes, avoiding sockets, minimizing all lead lengths, and proper power supply decoupling. The ground plane minimizes distributed capacitance and inductance which degrade high frequency performance.

The HA-5033 buffer should be placed in close proximity to the HI-5700 flash converter to minimize distributed capacitance which may limit bandwidth. Decoupling capacitors should also be placed close to the power and reference pins of the IC. Chip capacitors are preferred as they have the lowest lead inductance. When using both solid tantalum and ceramic capacitors the ceramic capacitors should be located nearest the IC pins for optimum high frequency decoupling followed by a solid tantalum capacitor optimizing low frequency performance. The decoupling capacitors must exhibit a low impedance from the sampling frequency up to the highest frequency component present.

A data latch is placed close to the HI-5700 to minimize capacitance on the data outputs. The digital power supply (VDD) transient currents can be exceptionally large due to dynamic current in the 8 digital outputs. If all bits change simultaneously and the rise/fall time of the outputs are 5ns and the load capacitance is 15pF, the resulting transient current is 120mA.

Placing an MDAC in the feedback path of an op amp or active filter, with the high-level signal tied to the V_{REF} pin and the I_{OUT} pin tied to virtual ground, permits digital control of gain or filter parameters.

Here, the Overflow bit of the HI-5700 ADC permits auto-ranging to be performed by feedback from the ADC's OFLO pin, through the μP to the level control DAC, reducing the gain by a fixed amount, and providing scaling information for the μP or DSP. Periodic logic controlled step increases in level permit slow AGC to compensate for changing conditions, such as light intensity shifts, with fast AGC action attenuating overloads. An EEPROM may be inserted in the data bus between the μP output and the DAC input for calibration or linearity adjustment.

HBC-10 Process Features

- **DIGITAL 5V CMOS**
  - 1.0μ L_{EFF}
  - Double Metal
  - Double Poly

- **ANALOG CMOS**
  - BVdss > 10V

- **ANALOG BIPOLAR**
  - 4GHz Std. 10V NPN
  - 3GHz HI-Beta (500) NPN
  - 1.3GHz PNP

- **PASSIVES**
  - Trimmable NiCr Resistor
  - Double Poly Capacitor
  - Zener Voltage Reference
  - Recessed Oxide Isolation

206651

HI5800
12-Bit, 3MSPS Sampling A/D Converter

- 3MSPS Sample Rate with No Missing Codes Over Temp
- 200ns Conversion Time
- 1.0 LSB Max Linearity Error Over Temp
- 20 MHz Full Power Input Bandwidth
- Buffered Track & Hold Amplifier
- ±2.5V Bipolar Analog Input Range
- 10MΩ Typical Input Resistance
- Precision 20ppm/°C Internal 2.5V Reference
- Low Power Dissipation: 1.8W Typical
- ±5V Supply Voltage
- Continuous or Single Shot Conversion Modes
- CMOS/TTL Compatible High Speed Digital I/O
- No Pipeline Data Latency

206652

60

Harris offers the HBC1000 BiCMOS cell based library for the Fast Track mixed-signal design system. BiCMOS features high integration with high performance. The HBC10 process combines precision bipolar transistors and passive components with high speed, high density CMOS devices. The list of active devices available on HBC10 is headed by an NPN transistor with a peak f_T of 4.5GHz and an emitter area of 1.4um by 1.4um. A 3GHz high beta NPN as well as a 1.3GHz vertical PNP are also available. Low voltage 1.0um channel length CMOS devices suitable for 5V operation as well as high voltage 2.0µm channel length devices intended for 10V operation.

Designers can choose between general purpose and high output impedance devices tailored for analog use among the 10V MOS devices. The list of passive components includes thin film laser trimmable NiCr resistors, double poly capacitors, a general purpose and precision buried layer zener diode, and a variety of diffused and implanted resistor structures. Circuit routing is accomplished by the two metal interconnect layers and the two polysilicon layers which form the MOS gates and capacitor plates.

The HI5800 is a monolithic, 12 bit, 3 MSPS BiCMOS sampling analog to digital (A/D) converter, fabricated in Harris Semiconductor's HBC10 BiCMOS process. It is a complete subsystem containing a sample and hold amplifier, precision 2.5V reference, two-step subranging 12 bit A/D, control logic, timing generator and digital I/O.

Designed for high speed applications where wide bandwidth and low power consumption are essential, the HI5800 conversion time is approximately 200ns with a throughput rate of 330ns (performance guaranteed over temperature with no missing codes). The converter features a high input impedance (>10MΩ) with bipolar analog input range of ±2.5V.

Intended applications include high speed data acquisistion systems, test equipment, communications, medical imaging, vibration analysis, waveform spectrum analysis, and CCD image scanners.

HI5800: A Complete Data Acquisition System on a Chip
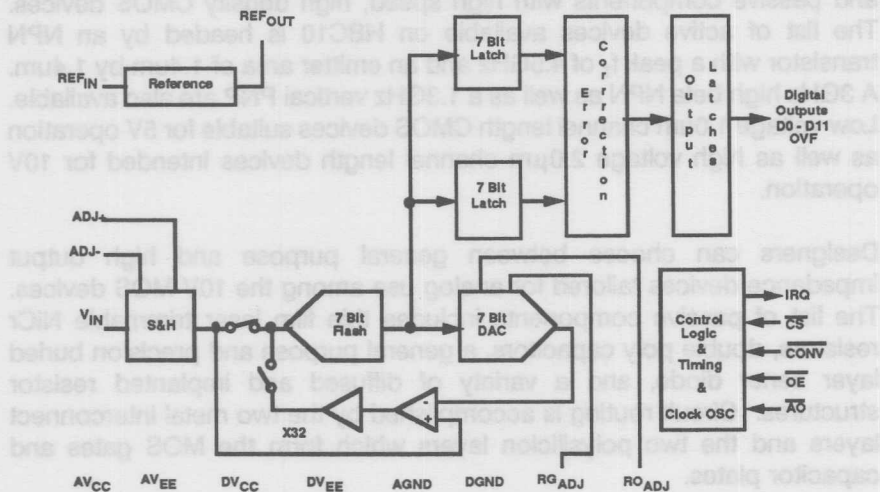
HI5800 FUNCTIONAL BLOCK DIAGRAM

206653

HI5800
12-Bit, 3MSPS Sampling A/D Converter
Typical Dynamic Performance

HI5800 ENOB vs fin

HI5800 SNR vs fin

HI5800 THD vs fin

HI5800 SFDR vs fin
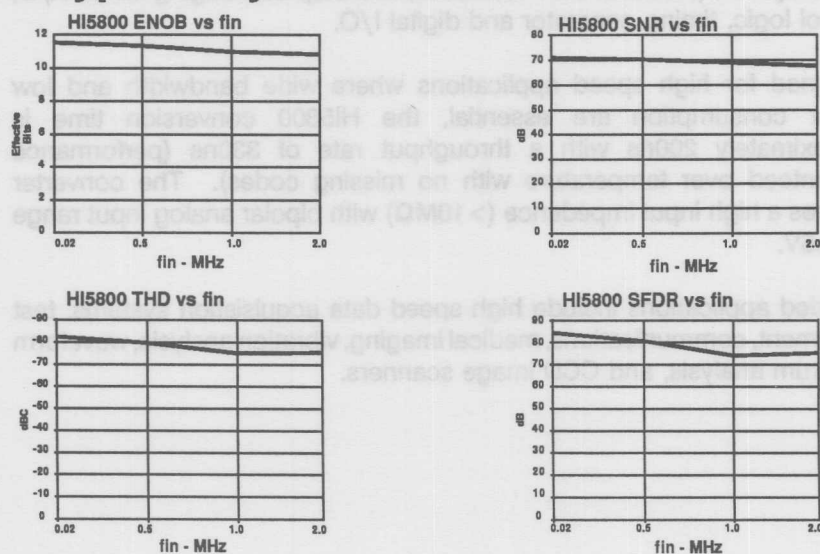
206654

The HI-5800 is a 12 bit sampling analog to digital converter which uses a subranging technique with digital error correction. The major system blocks illustrated in the block diagram are: sample and hold ampifier, 7 bit flash converter, precision reference, 14 bit accurate 7-bit R-2R D/A converter, error amplifier, digital error correction, and timing generator. The HI-5800 can be operated in either the single shot or the continuous convert modes.
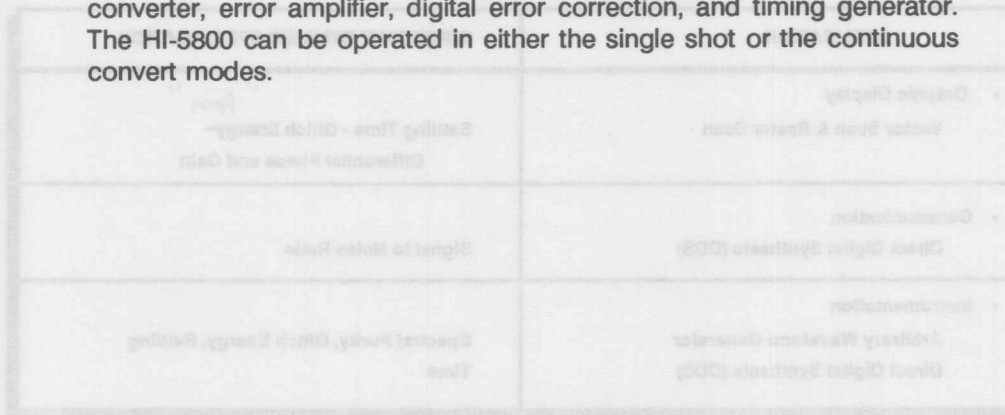
Excellent HI5800 performance beyond the Nyquist rate allows it's use as an undersampling converter with minimum degradation up to 3MHz input.

74dB is the theoretical signal-to-noise + distortion (SINAD) limit for an ideal 12 bit converter. Typical SINADs of 70.3dB and 69.5dB respectively are measured while sampling at 3MSPS w/20KHz and 1MHz sine wave inputs. For a 1MHz sine wave input, 11.25 effective number of bits is obtained.

Signal-to-noise ratio (SNR) is measured rms signal to rms sum of noise at a specified input and sampling frequency. Sampling at 3MSPS with 20KHz and 1MHz sine wave inputs, typical SNR is 72dB and 70dB respectively.

Total harmonic distortion (THD) is the ratio of the rms sum of the 2nd through 6th harmonic components to the fundamental rms signal for a given input and sampling frequency. At a 3MSPS sample rate with 20KHz and 1MHz sine wave inputs, typical THD measurements are -83.6dBc and -75dBc respectively.

Spurious-free dynamic range (SFDR) is the ratio of fundamental rms amplitude to rms amplitude of the next largest spur or spectral component. If harmonics are buried in the noise floor, it is the largest peak. For a 3MSPS sample rate with sine wave inputs of 20KHz and 1MHz, typical SFDR measurements are 80.2dB and 76.6dB respectively.

Selecting Proper D/A Converter for High Speed Application

APPLICATION	IMPORTANT DYNAMIC SPECIFICATION
• Graphic Display	
Vector Scan & Raster Scan	Settling Time - Glitch Energy *"Area"*
	Differential Phase and Gain
• Communication	
Direct Digital Synthesis (DDS)	Signal to Noise Ratio
• Instrumentation	
Arbitrary Waveform Generator	Spectral Purity, Glitch Energy, Settling
Direct Digital Synthesis (DDS)	Time

206655

Glitch Impulse Area

Data: 100.....0
Data: 011.....1
(Major carry translation)
1 LSB

A1, A2, A3, A4

Maximum Glitch Amplitude

Time Axis
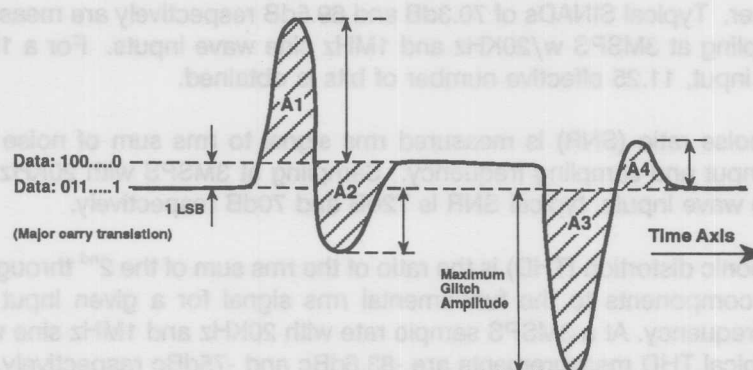
• A1, A2, A3, A4 Aberrant Areas Under the DAC Output Waveform

• Glitch Area Specification: Largest Net Area of (|A1| - |A2|) or (|A3| - |A4|)

• Glitch Area is expressed as "Voltage" Multiplied by "Time"

206656

64

A DAC must be specified not only for its DC characteristics (INL, DNL, Gain error...) but also for its AC characteristics and dynamic behavior which are application dependent. The dynamic characteristics of high speed DACs can be separated into 2 categories; time domain and frequency domain.

In graphic display systems, settling time and glitch energy are the important time domain specifications. The DAC output must settle well within a pixel period with a low transient glitch for a sharp, clear picture. The differential gain and phase are mixed time domain and frequency domain characteristics which are important in color TV systems and similar displays. The DAC should not show excessive gain and phase change for the high frequency color (chrominance) signal when the brightness (luminance) level changes.

Direct digital synthesis techniques (DDS) rely on a high speed DAC to convert a data sequence to an analog signal.

Glitch is a spike caused by an intermediate code generated for a short interval of time when DAC input is changing from one code to another. This is a result of internal timing skews between individual bits caused by asymmetrical digital propagation delays and DAC switch "on" and "off" switching time differences.   Normally, the worst case glitch occurs on the major carry transition which is from code 011..11 to 100..00 or vice versa. Note that the glitch produced by code transition between 011..11 to 100..00 is different from that produced by 100..00 to 011..11.

Linear filtering generally reduces the amplitude and increases the duration of the glitch impulse, resulting in the similar value of "amplitude" multiplied by "time". Track and hold amplifiers can be used as a deglitcher (nonlinear filtering) in lower speed DACs. However, as the resolution and speed of the DAC increases, deglitching using Track and hold amplifiers becomes impractical and the DAC itself should be designed for having a low glitch impulse area.

⊞ Glitch Impulse Effects

- **RASTER SCAN DISPLAY SYSTEMS:**

  Glitch Generates Pixel Color and Brightness Transient Changes Resulting in Ghost Patterns on the CRT.

  If DAC Is Used for Horizontal Sweep, Glitch Generates Vertical Strips Across the CRT.

- **VECTOR SCAN DISPLAY SYSTEMS:**

  Glitch Generates CRT Trace Aberration Resulting in a Distorted Display.

- **DIRECT DIGITAL SYNTHESIS:**

  Glitch Generates Harmonic Distortion When DAC Reconstructing a Sine Wave.

206657

⊞ Settling Time and Update Rate Specifications
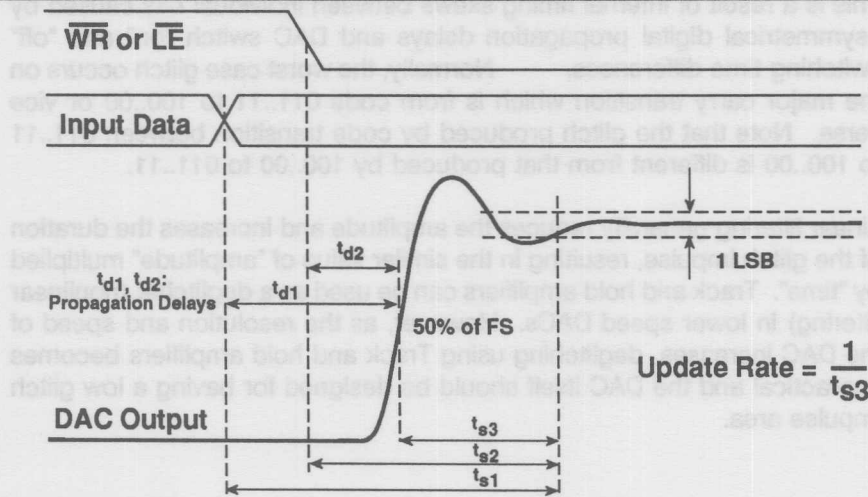
- t_{s1}: Settling Time Referred to Input Data Change (for DACs with No Input Register)
- t_{s2}: Settling Time Referred to Write or Latch Enable (for DACs with Input Register)
- t_{s3}: Settling Time Referred to DAC Output Eliminating the Propagation Delays

206658

In raster scan graphic display, DAC-generated glitches cause transient changes in brightness. Glitch impulses are one of the sources of harmonic distortion in signal generation.
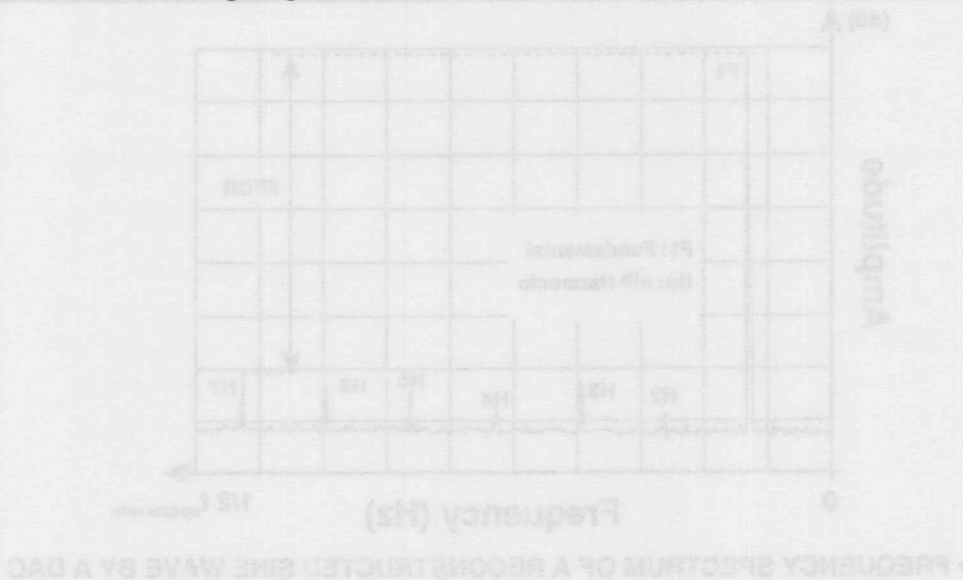
DAC settling time is the time between the digital input change and the output settling to a specified error band. The specified error band is normally ±1/2 LSB. However, for higher resolution DACs the error band may be increased to 1 or 2 LSB due to the difficulty of resolving 1/2 LSB in practical test circuits. The settling time is specified for fullscale output transition which is equivalent to all digital inputs changing from 0 to 1 or 1 to 0.

DAC Frequency Domain Specification

F1: Fundamental
Hn: nth Harmonic

• FREQUENCY SPECTRUM OF A RECONSTRUCTED SINE WAVE BY A DAC

206659

DAC Frequency Domain Specification

• **SFDR: Spurious-Free Dynamic Range Is the Ratio of the Fundamental RMS to the RMS of the Largest Harmonic, Spur or Noise Component.**

• **nth Harmonic Distortion: Ratio of the nth Harmonic to Fundamental**

• **THD: Total Harmonic Distortion**

$$THD_{dBc} = 20 \log \sqrt{Antilog \, (H2_{dBc}/10) + Antilog \, (H3_{dBc}/10) + \ldots\ldots}$$

• **SNR: Signal to Noise Ratio Is the Ratio of the Fundamental RMS to the Total Noise RMS In the Bandwidth of Interest.**

• **SINAD: Signal to Noise Plus Distortion Ratio**

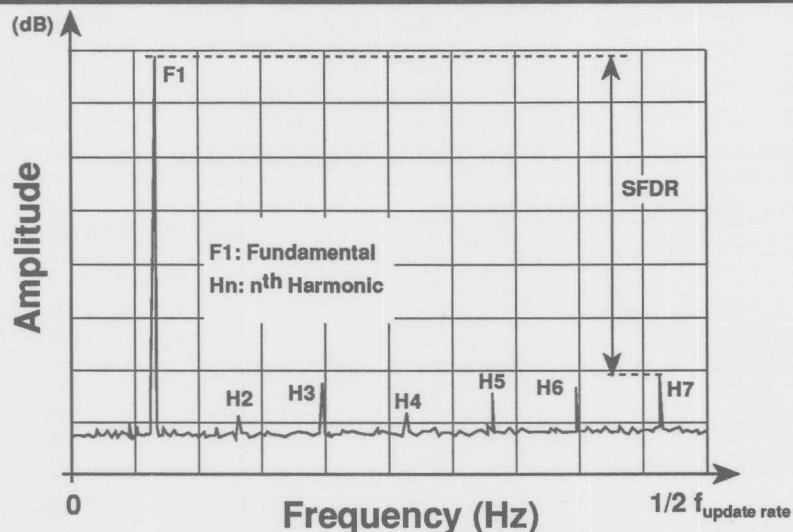$$SINAD = -20 \log \sqrt{Antilog \, (-SNR_{dBc}/10) + Antilog \, (THD_{dBc}/10)}$$

206660

DAC frequency domain specifications are expressed as a ratio of the desired signal (fundamental frequency) power or RMS value and the undesired signal's (harmonics, noise) power or RMS value. These ratios are specified in dBc, the ratio in dB referenced to carrier frequency.

The spurious free dynamic range (SFDR) specification is intended to quantify the usable dynamic range, the range in which frequency components other than the fundamental do not exist. It indicates the largest harmonic, spur or noise component. This is usually one of the harmonics. However, if the harmonics are down to the noise floor and indistinguishable then the highest spur or noise will be considered.

Total harmonic distortion (THD) is the ratio of the RMS sum of all the harmonics to the RMS of the fundamental signal. If individual harmonic distortions are measured in dBc then the THD can be calculated as shown. THD should consider all the harmonics; however, 1/2 the update rate frequency is the highest logical limit for harmonics to be regarded. If a reconstruction filter with a lower bandwidth is used at the DAC output, then higher number harmonics can be eliminated from the calculation.

Signal to noise ratio plus distortion (SINAD) or the classical definition of the SNR is the ratio of desired signal to total unwanted signals in the desired bandwidth. Having SNR and THD in dBc, SINAD can be derived as shown.
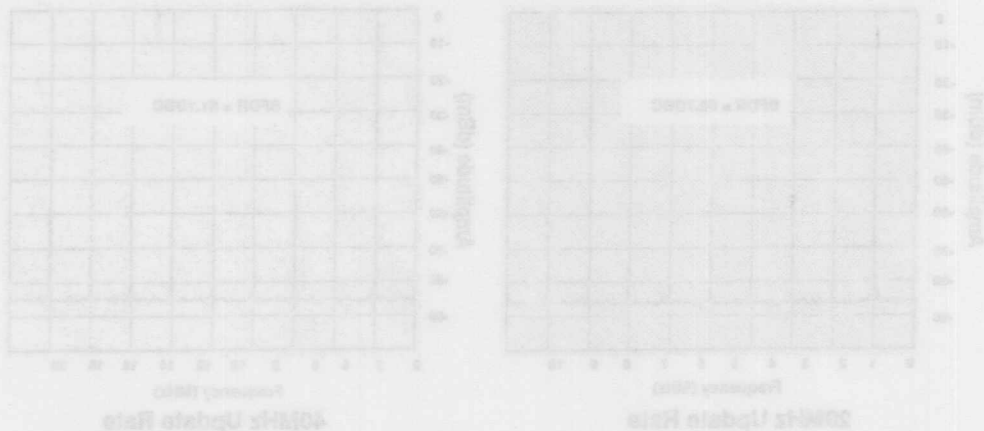
CA3338 CMOS 8-Bit Video Speed DAC

- **FEATURES:**
  - **- CMOS/SOS Low Power**
  - **- Segmented Output for Low Output Glitch: 150pV - sec**
  - **- Fast Settling Time: 20ns to 1/2 LSB**
  - **- High Update Rate: 20MHz (Guaranteed), 50MHz (Typical)**
  - **- Unipolar and Bipolar Output**
  - **- CMOS and TTL Compatible Digital Inputs**
  - **- Voltage Output**
  - **- R - 2R Architecture**

206662

CA3338 Frequency Domain

20 Data Points/Cycle Reconstructed Sine Wave

SFDR = 52.7DBC

20MHz Update Rate

SFDR = 51.1DBC

40MHz Update Rate
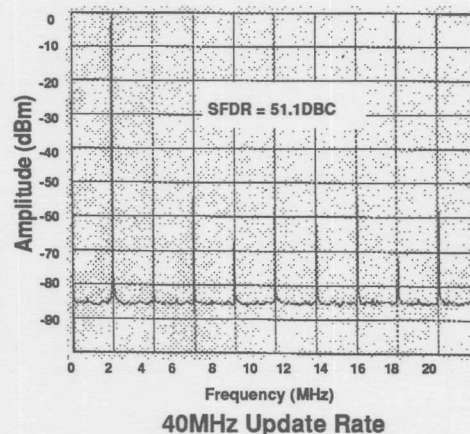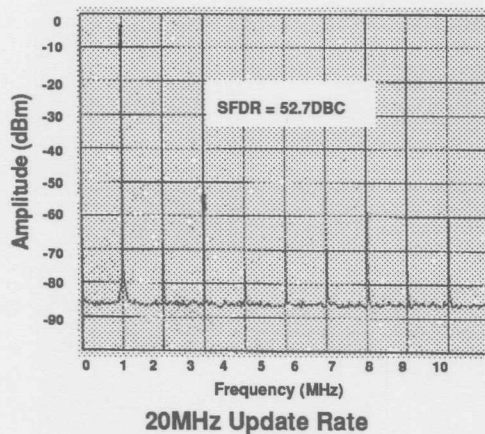
206663

The CA3338 is a high speed voltage output R-2R architecture DAC. It operates from a single 5V supply at video speed. The CA3338 is manufactured on a sapphire substrate which gives low dynamic power dissipation, low output capacitance and inherent latch-up resistance.

CA3338 output frequency response is shown here at 2 update rates (20MHz and 40MHz). The fundamental output frequencies are 1MHz and 2MHz. In each case, the same 20 data points are used.
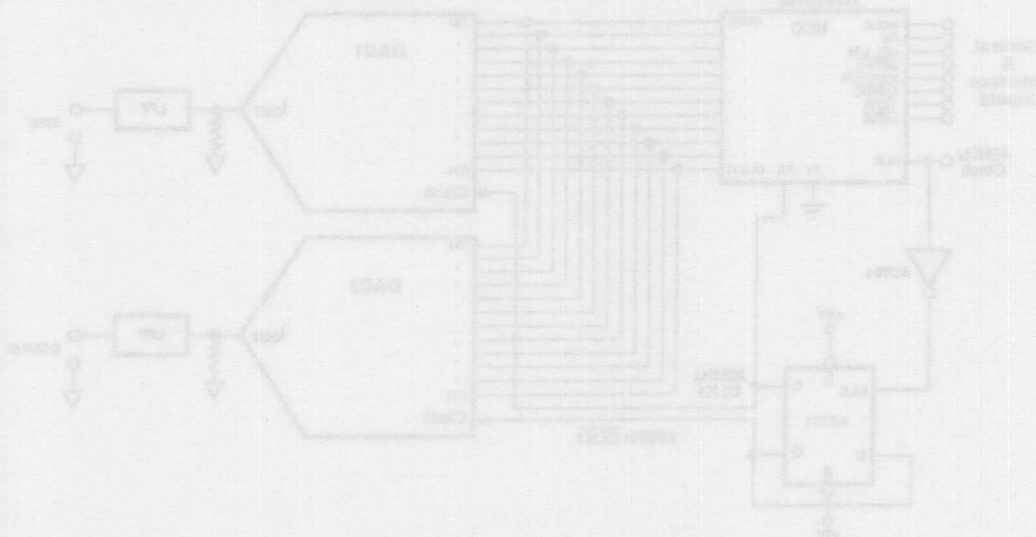
CA3338 at 20MHz & 40MHz Update Rate

20 Data Points/Cycle Reconstructed Sine Wave
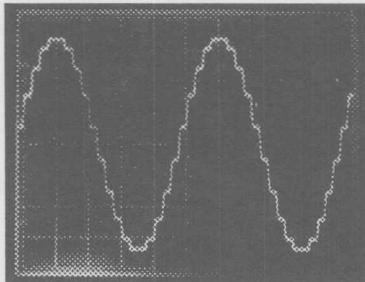
20MHz Update Rate

f_{OUT} = 1MHz

Measurement BW = 20MHz

Vert.: 0.1V/Div, Horz.: 200ns/Div
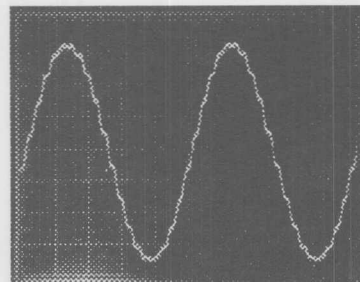
40MHz Update Rate

f_{OUT} = 2MHz

Measurement BW = 20MHz

Vert.: 0.1V/Div, Horz.: 100ns/Div

• DAC DRIVING A DOUBLY TERMINATED 50Ω CABLE

206664

Direct Digital Synthesis (Sine/Cosine)
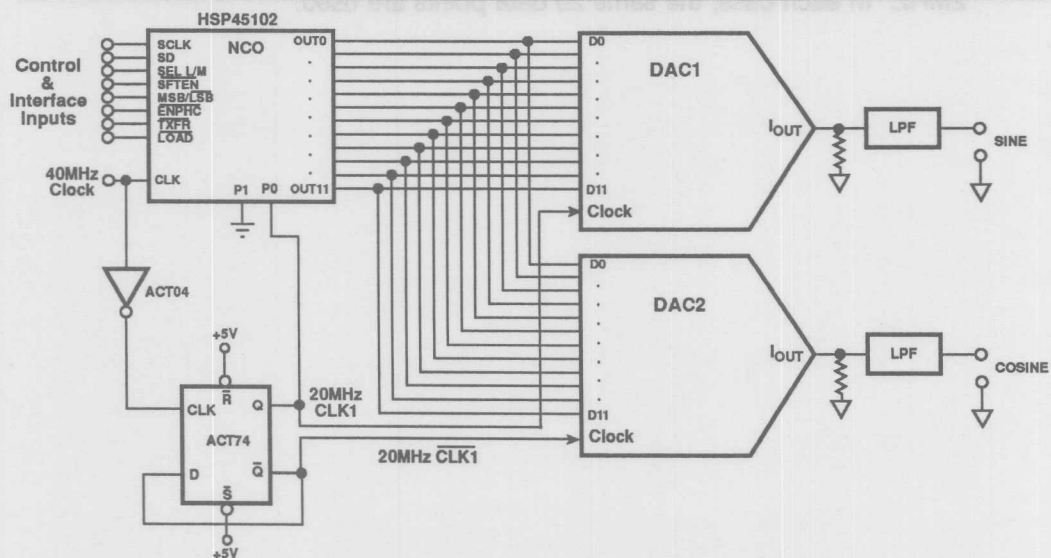
206665

Shown here are CA3338 outputs in the time domain reconstructing a sinewave with 20 data points/cycle at update rates of 20 and 40MHz. The pictures correspond to the frequency spectrums of the previous figures.

The CA3338 directly drives a doubly terminated 50 Ohm cable for these measurements and produces a 0.7 volt pk-pk output. These measurements were made using a 20MHz low pass filter.
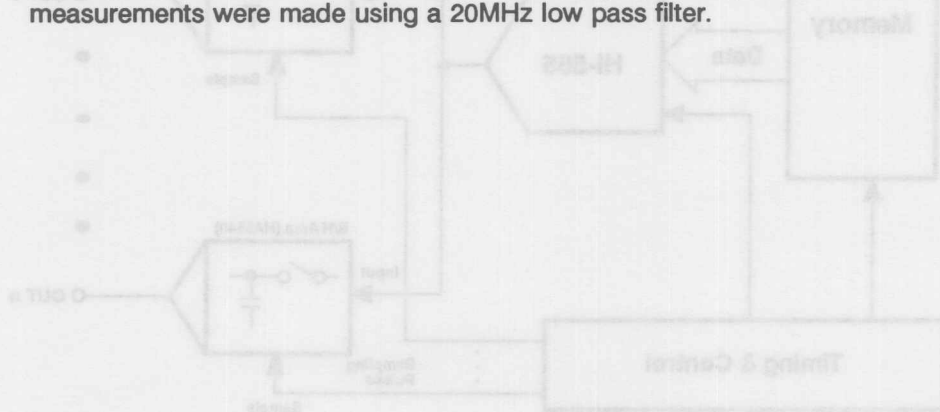
This circuit uses one numerically controlled oscillator (NCO) and two DACs to generate sine and cosine waveforms. This is traditionally implemented using 2 NCOs and 2 DACs or more complicated NCOs with both outputs.

Sine/cosine waves of the same frequency have many applications in communications and signal processing. The NCO12 provides P0 & P1 inputs which can modulate the phase shift of the output data sequence for phase shifts of 0, 90, 180 and 270 degrees.

![Harris Semiconductor logo] HARRIS
SEMICONDUCTOR
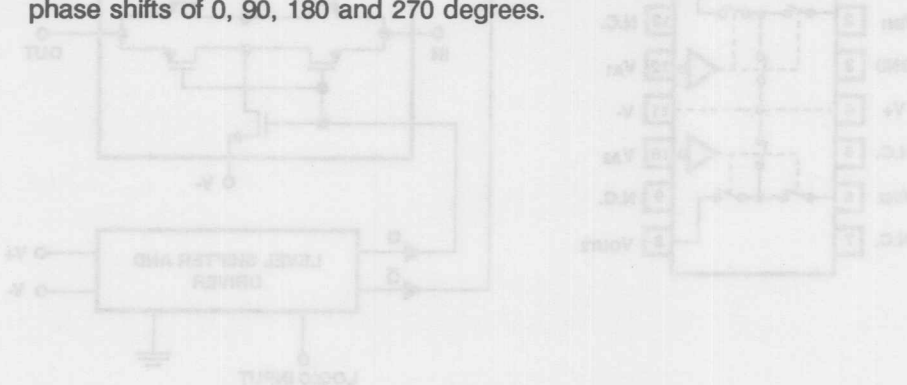
Multiple Output Signals from Single DAC
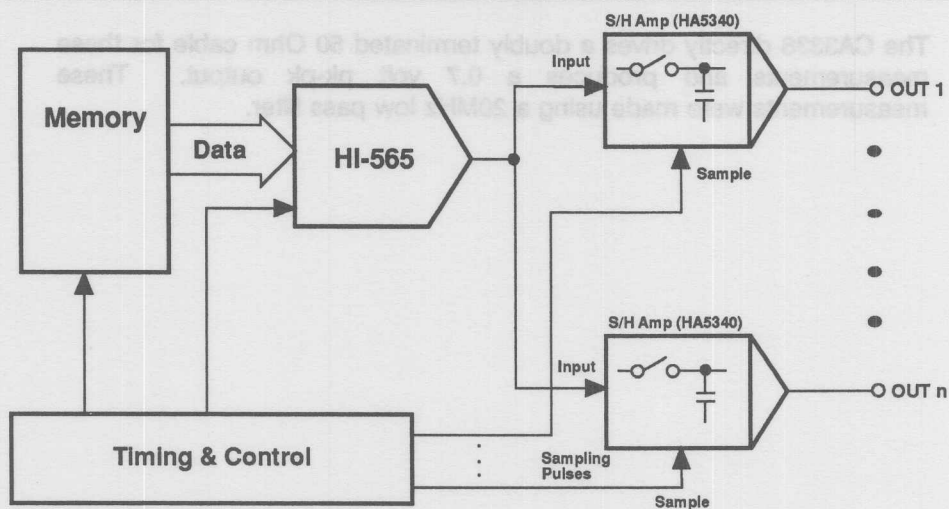
206668

HI-222 Video Switch
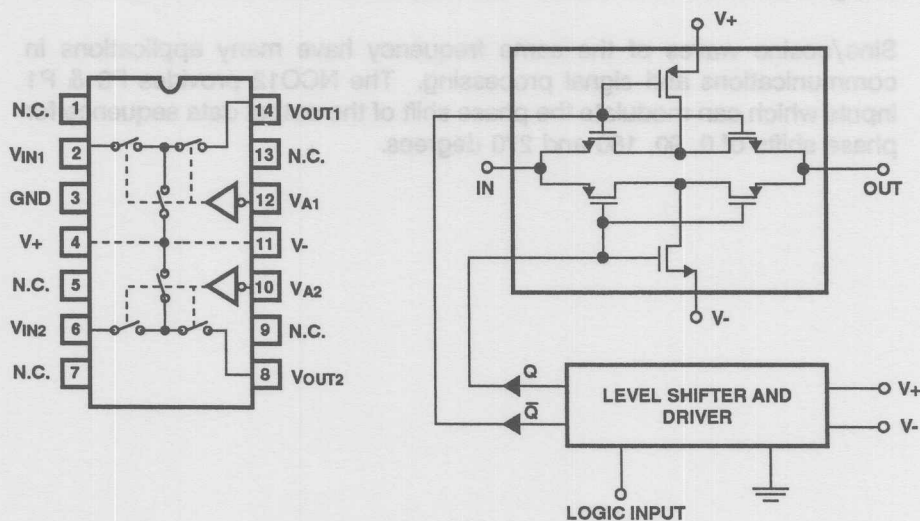
206669

A DAC can be used along with a large set of sample and hold amplifiers to generate multiple outputs. In this application the limiting factor of the maximum speed is the acquisition time of the sample and hold amp rather than the settling time of the DAC. The HA5340 has an acquisition time of 700ns to 12-bit accuracy (0.02%).

The HI-222 is a dual SPST analog switch. With a bandwidth greater than 200 MHz, the HI-222 has the range to satisfy the requirements of imaging systems, high definition television (HDTV), ultrasound and sonar.

"T" switch analog sections provide optimum Off Isolation and Crosstalk performance. Excellent differential gain and phase specifications allow color signals to be switched with minimal degradation.

HARRIS
S E M I C O N D U C T O R

HI-222 Dual High Frequency Video Switch

- **FEATURES**
  - Wide Bandwidth. 200MHz
  - Low Differential Gain 0.03%
  - Low Differential Phase . . . . 0.003°
  - Low R_{ON} 35Ω
  - High Off Isolation @ 10MHz 65dB
- **APPLICATIONS**
  - Routing Switches
  - Production Mixers
  - High Definition TV

206670

HA-2444
Selectable, Four Channel Op-Amp

- **FEATURES**

- Digital Selection of Input Channel	- 45MHz Unity Gain Bandwidth
- 160V/μS Slew Rate	- 60nS Channel Selection
- 0.03% Differential Gain	- 0.03° Differential Phase
- 0.1dB Gain Flatness to 10MHz	- 60dB Crosstalk Rejection
- 76dB Open Loop Gain	

- **APPLICATIONS**
  - Special Effects Processors, Video Multiplexer
  - Medical Imaging Systems
  - Heads-up / Night Vision Systems

206670A

76

PC board layout is critical to maintaining isolation, with attention to stray capacitance, lead inductance and coupling: (See Application Note 559)

HA-2444 Operation

D0	D1	EN	OUT
X	X	L	NONE
L	L	H	CH1
H	L	H	CH2
L	H	H	CH3
H	H	H	CH4

- X = Don't Care
- When Disabled the Output is a High Impedance

206670B

Harris Semiconductor

COMMUNICATIONS

IMAGING

ATE

SIGNAL GAIN — X

SIGNAL CONDITIONING — ƒ(t)

ADC DRIVER

ANALOG to DIGITAL — 00110

DSP

DIGITAL to ANALOG — 00110

SIGNAL CONDITIONING — ƒ(t)

MULTIPLEX
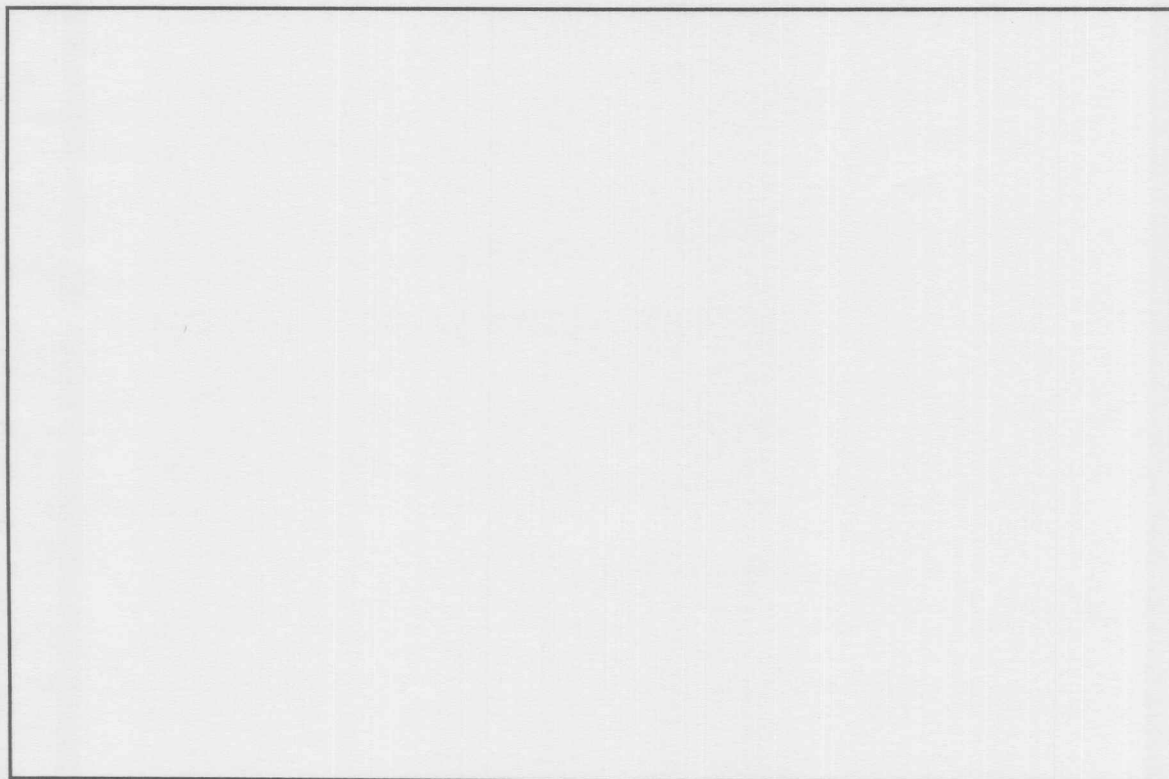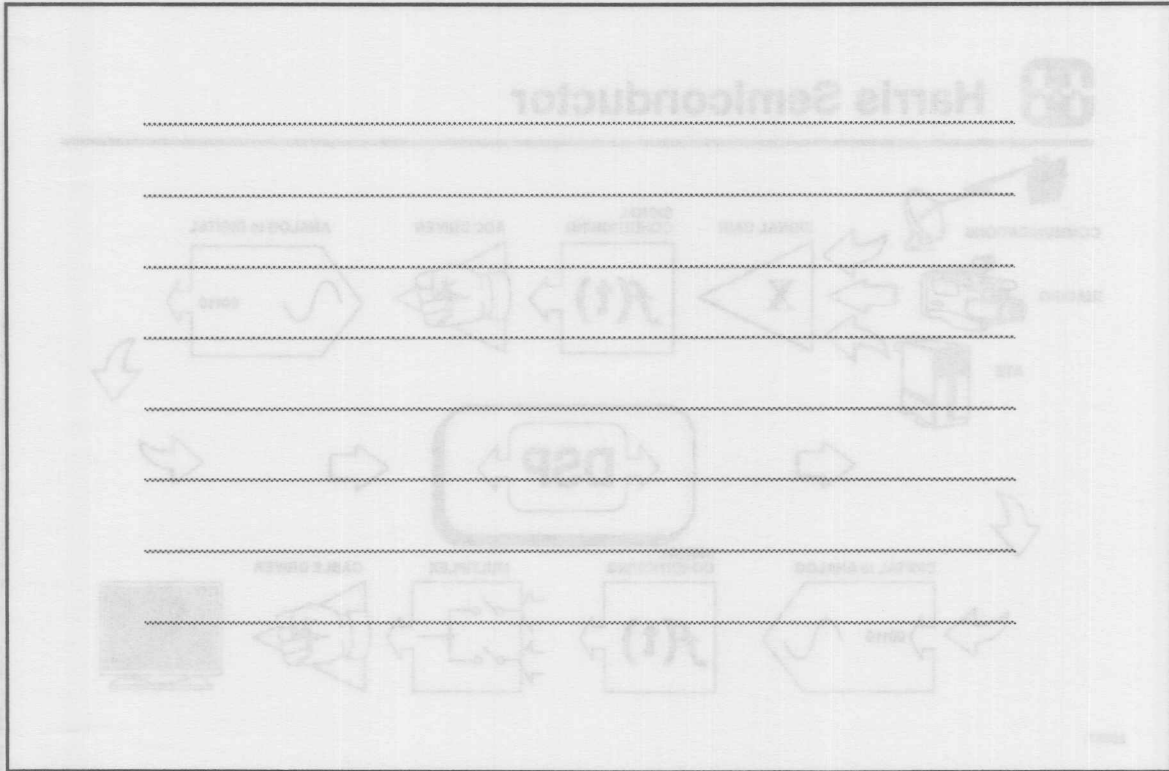
CABLE DRIVER
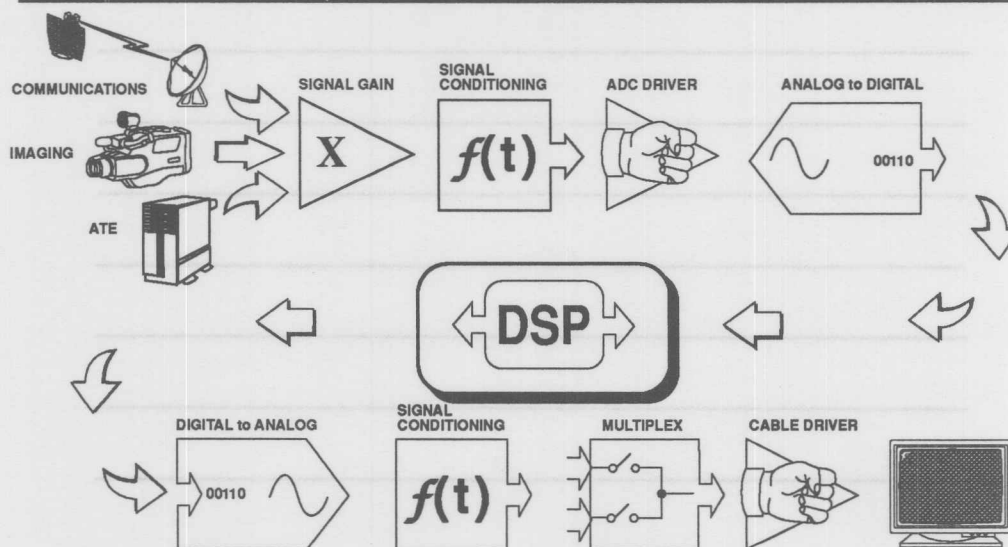
206671

DIGITAL
SIGNAL
PROCESSING

Transition to DSP

- MANY TRADITIONAL ANALOG DESIGNS ARE INCORPORATING DSP
- WHY???
  - Wide Dynamic Range
  - Digital is Immune to Drift in Component Values Due to Aging and Temperature
  - No Noise Due to Temperature Variation
  - Easy to Reprogram without Changing Hardware
  - Digital is Immune to Vibration (Microphonics)
  - New Functions are Possible

206672

Key Applications for DSP

- COMMUNICATIONS
  - Digital Receivers
  - Digital Transmitters
  - Satellite Ground Stations
  - Cellular Phone Cell Sites
  - Modems
  - Frequency Synthesizers
  - Telemetry
  - Navigation and Guidance
- INSTRUMENTATION
  - Spectrum Analyzers
  - Digital Oscilloscopes
  - Simulators
  - Digital Test Equipment
- IMAGE & VIDEO PROCESSING
  - Ultrasound
  - Image Enhancement
  - Machine Vision
  - Broadcast Video
  - Special Effect Video
  - Accelerator Boards
  - Document Scanners
  - Target Acquisition
  - Surveillance Systems
  - Automatic Inspection
  - Feature Extraction

206673

As system performance demands increase, traditional analog solutions are being replaced by DSP. DSP allows a user to design a system with a dynamic range that is difficult to achieve using analog techniques (90 dB or greater) and is inherently immune to many of the problems associated with analog electronics. In addition, the use of digital signal processing enables new types of products to become commercially practical, such as spread spectrum communications, ultrasound and machine vision.

DSP usage is expanding across many markets and applications. With increasing levels of integration and decreasing costs, high performance DSP is moving out of the strictly military marketplace and finding its place in commercial and consumer products. Harris is making high performance DSP a cost effective solution for this end of the market. We are concentrating on three areas, which are shown here: communications, instrumentation and image processing. Some of the target applications we are focusing on are shown in each of the three types of products.

Harris DSP Products

COMMUNICATIONS / INSTRUMENTATION

HSP45116	Numerically Controlled Oscillator / Modulator
HSP43220	Decimating Digital Filter
HSP45102	12-Bit Numerically Controlled Oscillator
HSP45106	16-Bit Numerically Controlled Oscillator

GENERAL PURPOSE DSP FUNCTIONS

HSP45240	Sequencer
HSP43168	Dual Digital Filter
HSP45256	Correlator
HSP43481, HSP43881, HSP43891	Digital Filters
ISP9520/1	Pipe Line Delay
HMU16, HMU17, HMA510	Multipliers/MAC

2d sourced. (handwritten)

IMAGE & VIDEO PROCESSING

HSP48908	Two Dimensional Convolver
HSP48901	Image Filter
HSP9501	Row Buffer
HSP48410	Histogrammer / Accumulating Buffer

206674

Digital Receiver

DIGITAL CHANNELIZER

HSP45116 NCOM   HSP43220 DDF

LO — LOW PASS FILTER — A/D — COMPLEX DOWNCONVERTER — LOW PASS FILTER → 16-BIT REAL / LOW PASS FILTER → 16-BIT IMAG.

PHASE/FREQ CONTROL   DECIMATION CONTROL
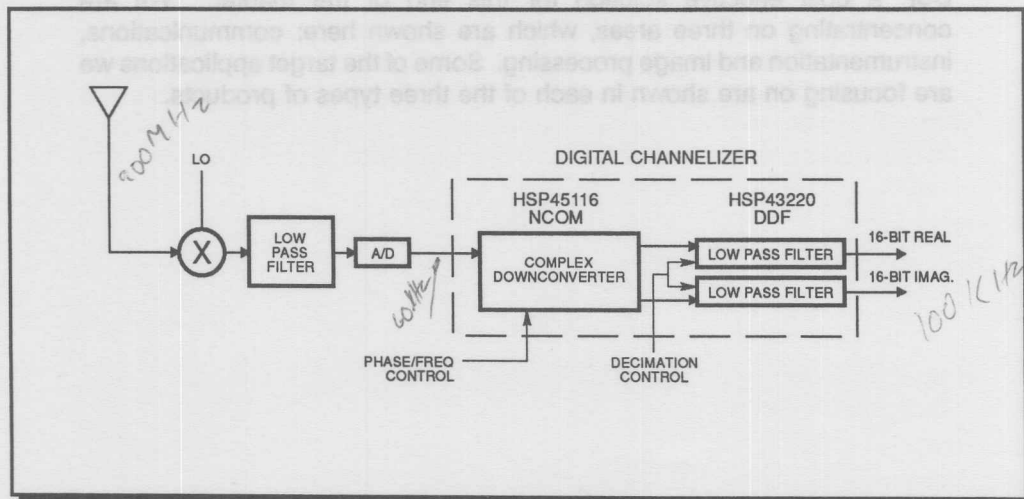
206675

The products shown were designed to perform specific functions in each application and to answer a specific system need. Often those systems are now answering their needs using analog electronics for preprocessing and a DSP microprocessor on the back end. They rely on the analog electronics to filter out most of the data so that the microprocessor can operate on the incoming information at a reduced data rate.

The disadvantage of this method is that the system is saddled with the nonlinearities noise and other weaknesses of the analog design, and only able to take advantage of DSP once the signal is at a very low data rate. To get around this problem, many systems are now using several microprocessors in parallel. Not only does this solution require a large amount of board space, but the designer has to deal with the problems of task partitioning and synchronization. Often, these microprocessors are performing repetitive tasks such as filtering, correlation, or sine wave generation, which is a waste of their power and programmability.

Alternatives to DSP microprocessors include a set of single chip solutions such as these that either replaces some of the analog electronics or replaces the DSP microprocessors that are performing repetitive tasks. Since the work of many microprocessors is now being performed on a single chip, the user saves money, real estate and design time.

A basic function now possible with high performance DSP is the digital receiver. This circuit finds its way into the front end of radios, ultrasound sensors and other systems that receive a high frequency signal. In this diagram, the digital tuner block shown performs the equivalent function of the analog local oscillator, mixer and low pass filter in the front end. In the digital tuner, the HSP45116 generates the local oscillator, splits it into sine and cosine and mixes it with the incoming signal. The HSP43220s low pass filter the resulting signals to produce the base band real and imaginary (I and Q) signals on the output. The output signal could then be sent to a microprocessor, which would perform demodulation, signal extraction, etc.

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SEMICONDUCTOR

NCOM vs. VCO and Mixer

NCOM

Real

Data Input

Imaginary

Real Data Output

Imaginary

COS   SIN

Frequency and Phase Control

NCO
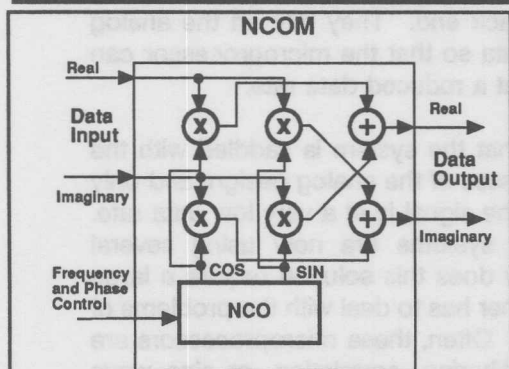
- Highly Precise Frequency and Phase Control
- High Spurious Free Dynamic Range
- Low Real/Imaginary Channel Mismatch
- Low Phase Noise
- Fast Frequency, Phase Changes
- Limited Tuning Range
- Performance Limited by A/D, D/A

VCO and Mixer

Input Signal

Frequency Control Voltage

VCO

∠90°

I

Output Signal

Q
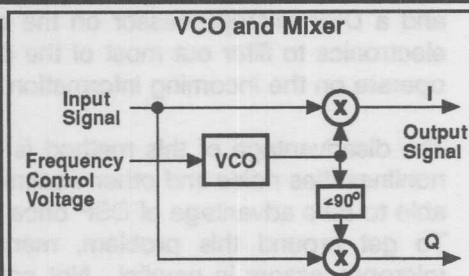
- Frequency and Phase Relatively Inaccurate
- Subject to Noise due to Temperature, Matching, Crosstalk
- Slow Frequency and Phase Changes
- Wide Tuning Range
- No conversions necessary (A/D, D/A)

206676

HSP45116 Numerically Controlled Oscillator-Modulator

- **33MHz SAMPLE RATE**
- **16 BIT COMPLEX INPUT**
- **20 BIT COMPLEX OUTPUT**
- **90dB SPECTRAL PURITY**
- **0.01Hz FREQUENCY RESOLUTION**
- **32 BIT FREQUENCY CONTROL**
- **16 BIT PHASE MODULATION**

DATA INPUT

16   16

PHASE   16
FREQ   32
CLOCK

CONTROL

LOOK UP TABLE

SIN

COS

COMPLEX MULTIPLY ACCUMULATOR

20   20

MODULATED OUTPUT

FUNCTIONS

FM   PSK

FSK   AM

COMPLEX DOWN CONVERSION

QAM

206677

86
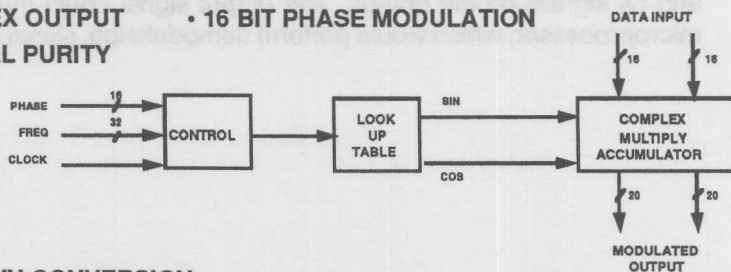
The advantage of performing the receiver function digitally is that we get the full benefit of the control and precision possible with digital electronics. The NCOM implements the function of an analog quadrature VCO and a pair of mixers. The digital implementation gives the user high resolution, low noise and precise phase matching at the cost of a limited input frequency range. The 30 to 40 MHz sampling frequency results in a maximum signal frequency of 10-15 MHz as opposed to the hundreds of MHz that are possible with the analog solution. With the process development currently under way, this gap will narrow in the near future.

The digital circuit also puts additional demands on the performance of the A/D converter in front of the NCOM. However, A/D technology is rapidly improving to the point where there are several viable alternatives to this part of the system.

The HSP45116 offers the user the precision of digital synthesis with the capability to mix an input signal. It has 32 bit frequency resolution, which produces an carrier frequency with an accuracy of .008 Hz. The look up table calculates the sine and cosine of that phase angle. Together these two blocks form what is known as a Numerically Controlled Oscillator, or NCO - the digital equivalent of a VCO and phase splitter. In the case of the NCOM, the NCO portion also has control pins that allow the user to change the frequency and phase of the sinusoid in a single clock cycle. These pins are designed to ease the implementation of many popular transmitter and receiver functions: FM, FSK, PSK modulation and demodulation, frequency hopped transmitters and receivers, and others.

The sine and cosine are generated simultaneously on every clock. The 16 bit resolution gives better than .006 degrees of phase mismatch.

The complex multiplier/accumulator (or CMAC) performs a full complex multiply of the data input and the sine and cosine in a single clock cycle. The CMAC is the digital equivalent of two balanced mixers. Together with the frequency and phase control pins, the CMAC can be used to implement many other common modulation techniques (AM, QAM, etc).

Digital vs. Analog Methods

Wideband Spectrum (High Sample Rate)

Baseband Spectrum (High Sample Rate)

Baseband Spectrum (Low Sample Rate)
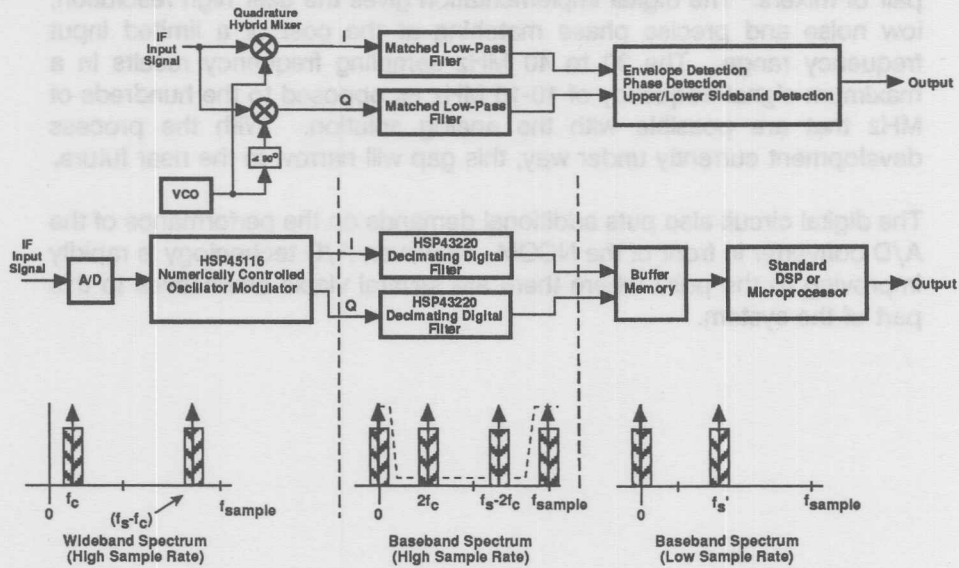
206678

Decimation - Reduction of Sample Rate

Time Domain   Frequency Domain

SIGNAL WITH INTERFERENCE

INTERFERENCE

SIGNAL OF INTEREST   SAMPLE RATE

FILTERED SIGNAL

FILTER RESPONSE

DECIMATED FILTERED SIGNAL

NEW SAMPLE RATE
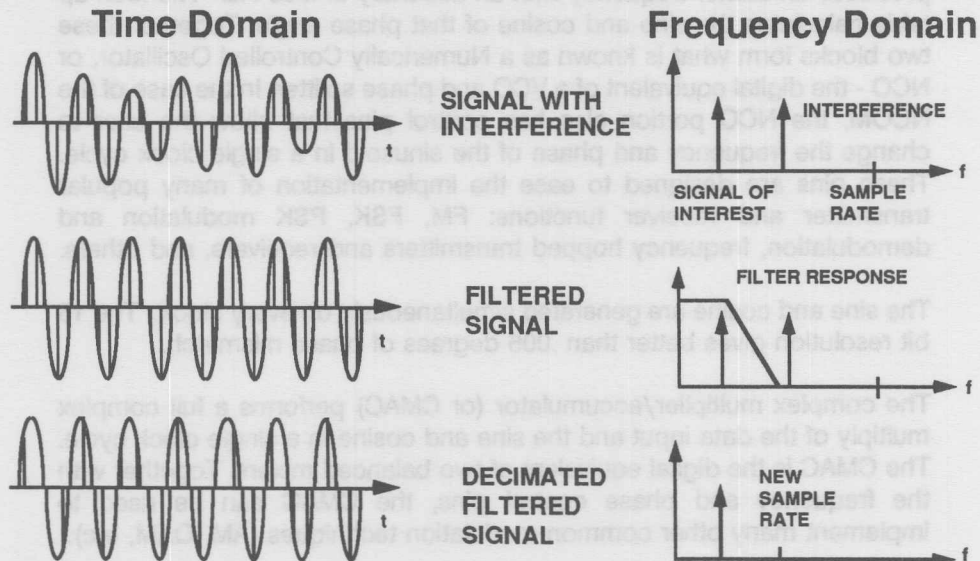
206678A

The HSP45116 and HSP43220 together form the digital equivalent to an analog tuner. The NCOM is the digital equivalent of a quadrature VCO with a pair of mixers, and the Decimating Digital Filter is a narrow band low pass filter. This chip set takes a wide band signal at a high sample rate, pulls a narrow band of information out of it and outputs that narrow band at a low data rate so that it can be analyzed by a microprocessor.

When comparing the digital solution to the analog, the advantages of the digital solution become apparent. Using the NCOM and DDF, it is possible to pull out very narrow channels with adjacent channel attenuation that is extremely difficult to obtain using analog methods.

The key to the operation of the chip set is the high order of sample rate reduction, or decimation, that it performs. The idea is to eliminate all extraneous information so that the processor can operate on only the signal of interest. In this example, the sample rate of the incoming IF signal might be 10's of megahertz; after the signal of interest has been shifted to base band (DC) the DDF can discard the redundant samples with no degradation in the desired signal. The final sample rate is sufficient for a microprocessor to complete the demodulation and/or signal analysis.

Decimation

	TIME DOMAIN	FREQUENCY DOMAIN

Over Sampled
Tone

After
Decimation
x2

After
Decimation
x4
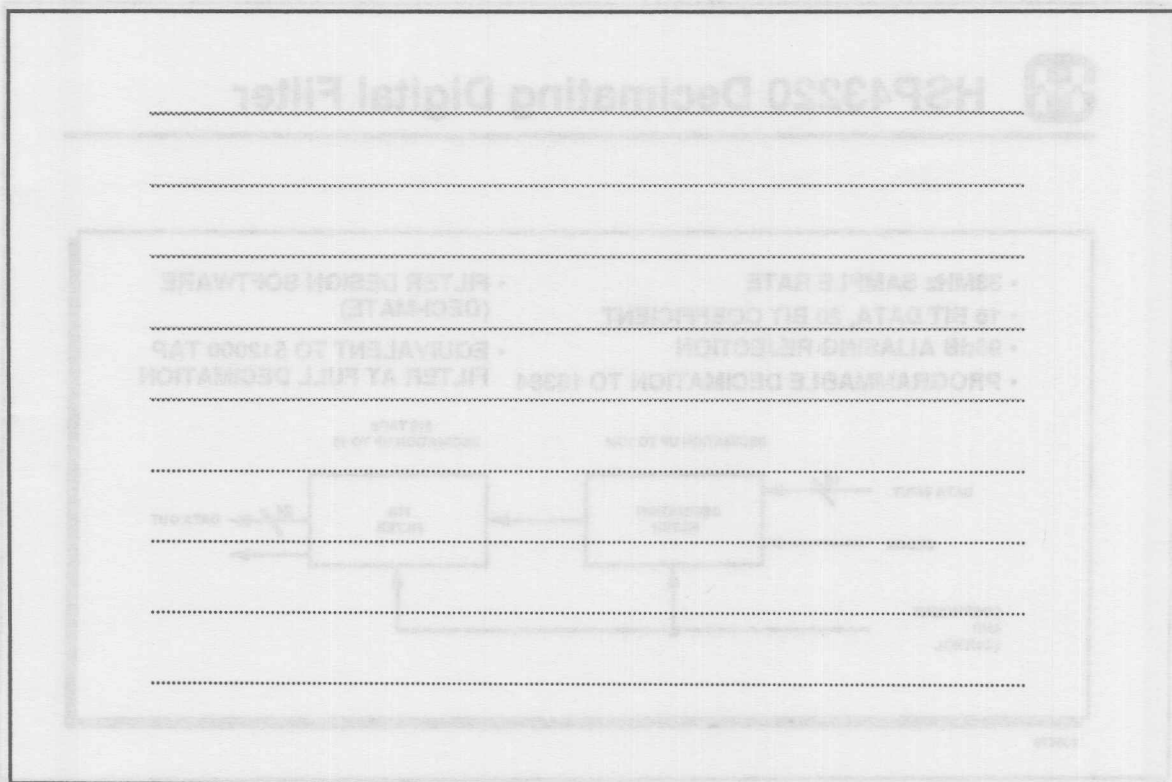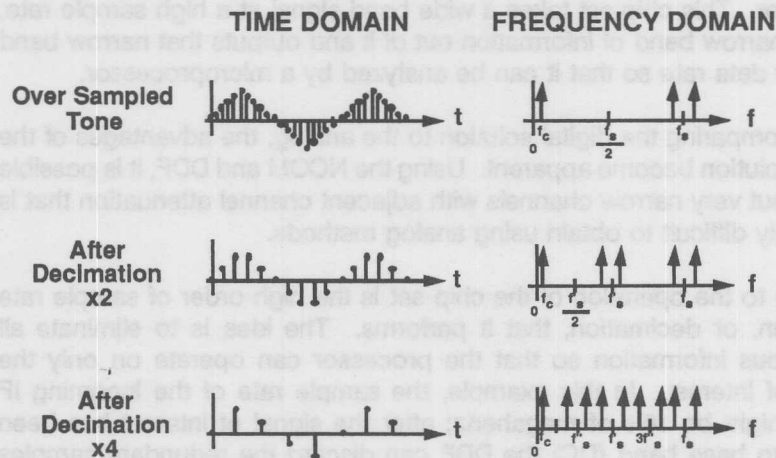
206678B

HSP43220 Decimating Digital Filter

- 33MHz SAMPLE RATE
- 16 BIT DATA, 20 BIT COEFFICIENT
- 96dB ALIASING REJECTION
- PROGRAMMABLE DECIMATION TO 16384

- FILTER DESIGN SOFTWARE (DECI-MATE)
- EQUIVALENT TO 512000 TAP FILTER AT FULL DECIMATION

DECIMATION UP TO 1024

512 TAPS
DECIMATION UP TO 16

DATA INPUT — 16 →
CLOCK →
DECIMATION
FILTER
→
FIR
FILTER
24 → DATA OUT

COEFFICIENT
AND
CONTROL

206679

90
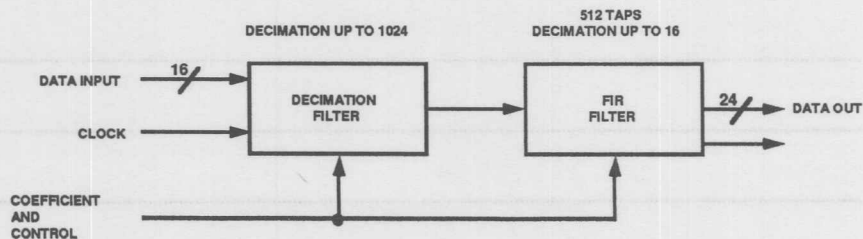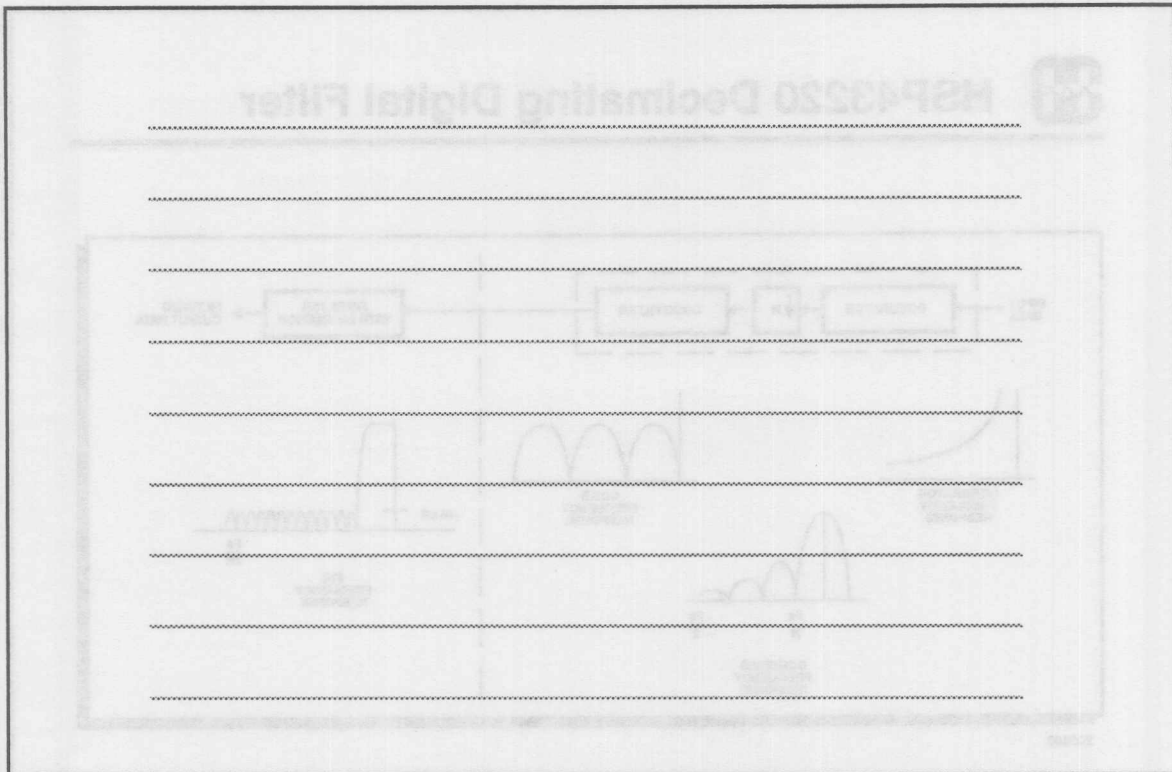
The Decimating Digital Filter is a two stage low pass filter designed to implement narrow band low pass filtering with high order decimation. It is a true finite impulse response (FIR) filter; the phase of the filter response is completely linear by design. The first stage (Decimation Filter) provides a first pass filter combined with high order decimation. The second stage filter is a programmable FIR filter which performs band shaping plus additional decimation. This combination yields a filter capable of pulling a narrow band signal out of a wide spectrum and decimating it so that the final signal is sampled at a rate consistent with the signal frequency.

The input data is 16 bits wide, while the output is 24 bits. All internal data paths maintain at least 16 bit accuracy. This fact together with the 20 bit coefficients in the FIR filter, provide the capability of 96 dB of attenuation of out of band signals. In reality, the actual attenuation obtained will depend on the parameters of the filter being designed; 96 dB is a good measure for many practical filters.

HSP43220 Decimating Digital Filter

INPUT DATA → INTEGRATOR → ↓R → COMB FILTER → FIR FILTER WITH DECIMATION → FILTERED OUTPUT DATA

INTEGRATOR FREQUENCY RESPONSE

COMB FREQUENCY RESPONSE

−96 dB

$\frac{Fs}{2R}$

FIR FREQUENCY RESPONSE

$\frac{Fs}{R}$ $\frac{Fs}{2}$

COMBINED FREQUENCY RESPONSE
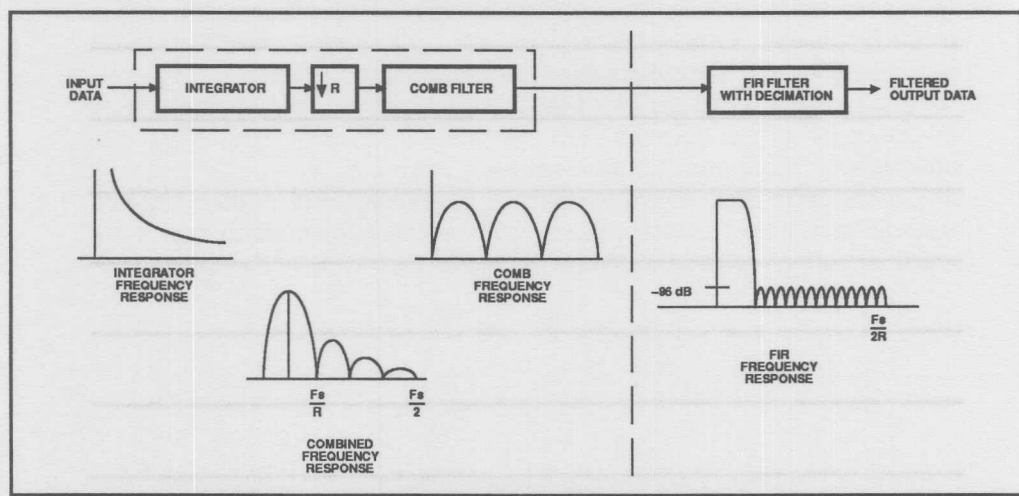
206680

Decimation of Wideband Signals

Decimation with Prefiltering

Low-Pass Filter

Noise

Signal

f

f_s
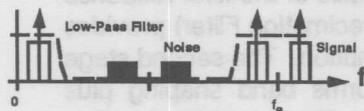
ORIGINAL WIDEBAND SPECTRUM W/FILTER CHARACTERISTIC

f

f_s
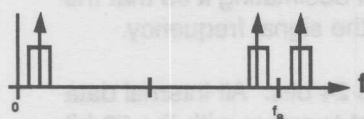
SPECTRUM AFTER FILTERING

f

f_s f_s
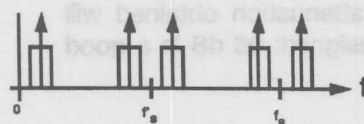
SPECTRUM AFTER DECIMATION

206680A

The first stage of the DDF consists of an integrator, decimator and comb. The combined response of all three has a frequency response in the form of a sinc squared function. Note that the nulls in the frequency response occur at the multiples of the decimated sample rate.

The second stage FIR provides a narrow band low pass filter on the output of the first stage. On a relative scale, the pass band of the FIR is much narrower than the central lobe in the response of the HDF. Since the sample rate of the FIR is Fs/R, the aliasing due to the decimation occurs at the nulls in the response of the first stage, so it gets maximum attenuation. When the two are combined, the result is that only a narrow frequency band around DC is passed; everything else is attenuated. A brute force solution to this would require a filter thousands of taps long, which would be extremely difficult to design.
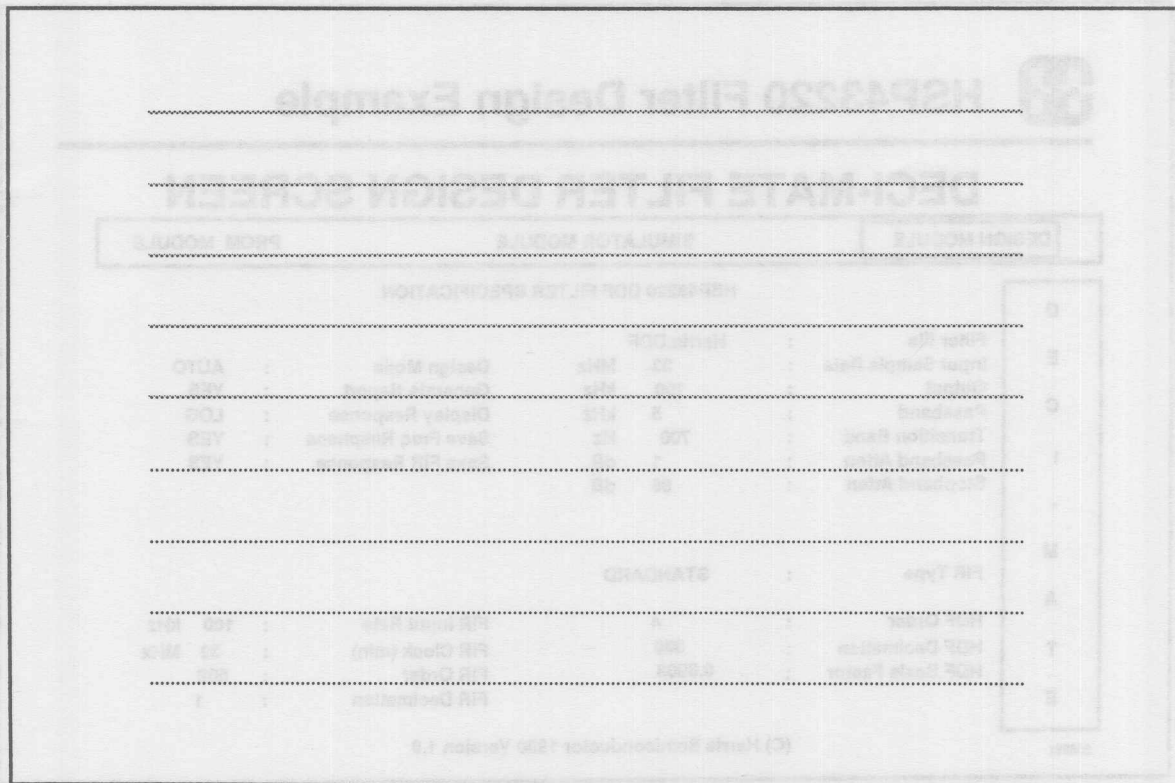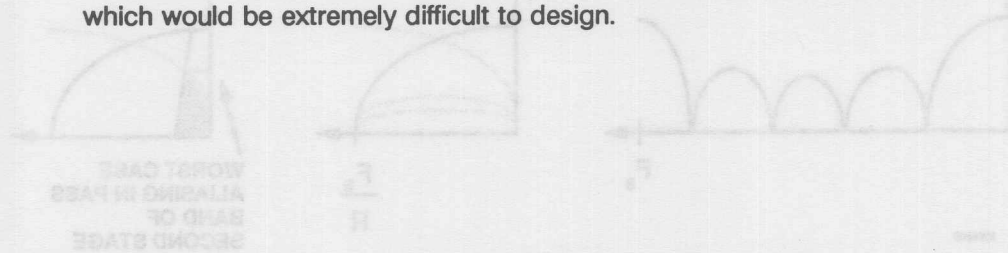
Two Filters Are Better Than One

1ST STAGE FILTER   DECIMATION   2ND STAGE FILTER

FILTER RESPONSE

ALIASING

F_s

$\dfrac{F_s}{R}$

WORST CASE ALIASING IN PASS BAND OF SECOND STAGE

206680B
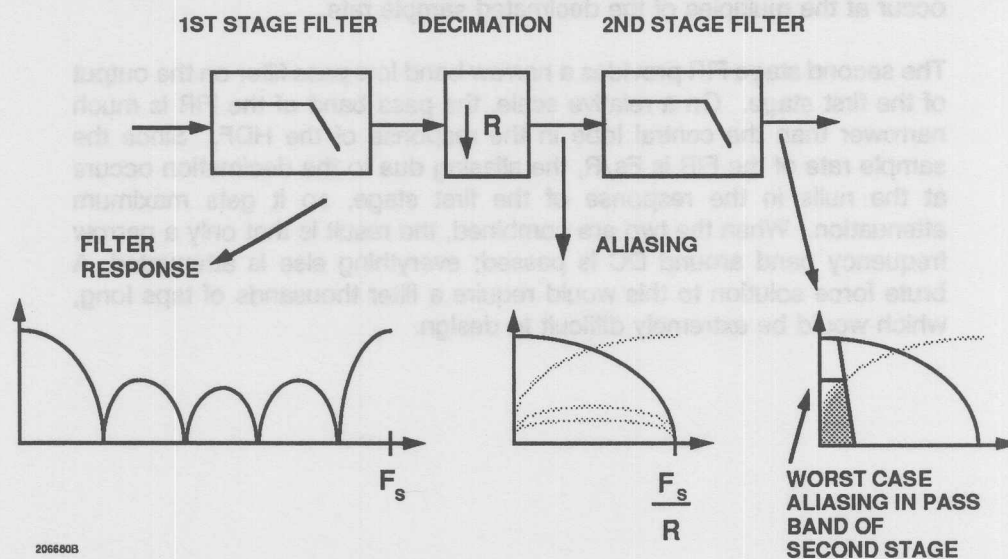
HSP43220 Filter Design Example

DECI•MATE FILTER DESIGN SCREEN

DESIGN MODULE	SIMULATOR MODULE	PROM MODULE

HSP43220 DDF FILTER SPECIFICATION

D
E
C
I
•
M
A
T
E

Filter file	:	Harris.DDF			
Input Sample Rate	:	33	MHz	Design Mode	: AUTO
Output	:	100	kHz	Generate Report	: YES
Passband	:	5	kHz	Display Response	: LOG
Transition Band	:	700	Hz	Save Freq Respnses	: YES
Passband Atten	:	1	dB	Save FIR Response	: YES
Stopband Atten	:	96	dB		

FIR Type	:	STANDARD			
HDF Order	:	4		FIR Input Rate	: 100 kHz
HDF Decimation	:	330		FIR Clock (min)	: 33 MHz
HDF Scale Factor	:	0.6903		FIR Order	: 509
				FIR Decimation	: 1

(C) Harris Semiconductor 1990 Version 1.0

206681
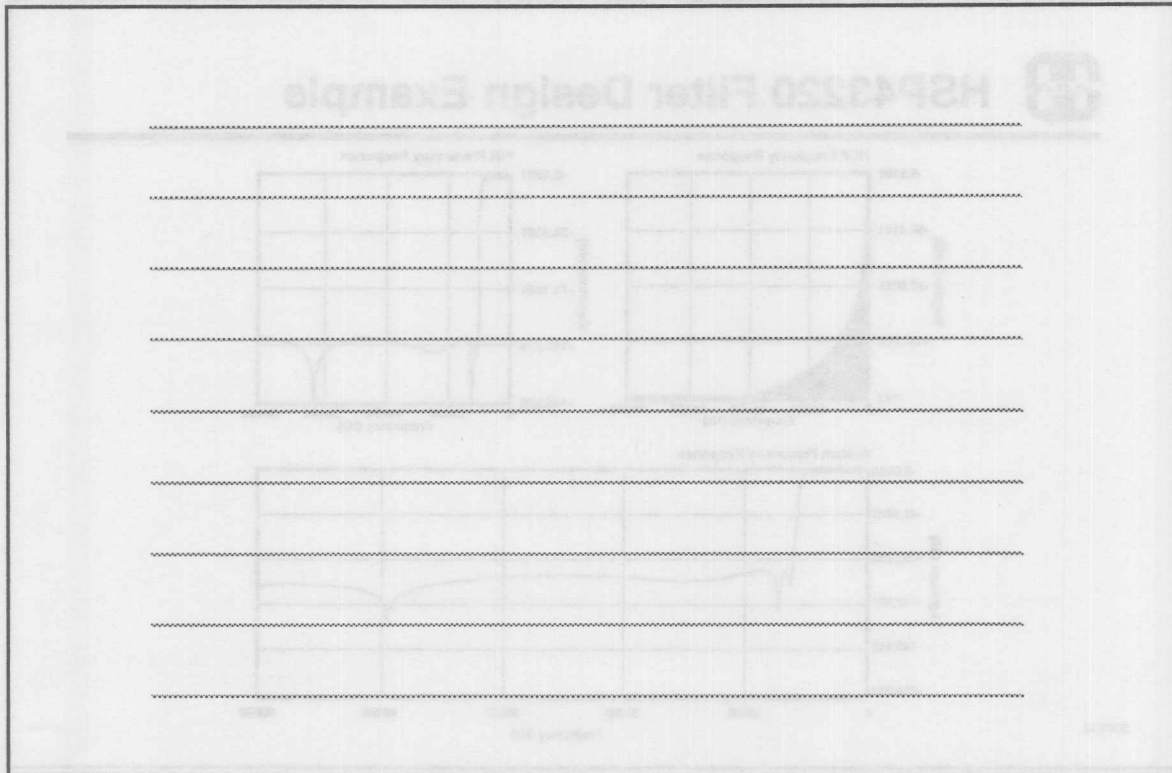
Since the DDF has a unique architecture, Harris provides special software to design the filter. This software takes the same parameters that would normally be provided to a standard FIR design program: input and output sample rate; the width of the pass band and transition band, pass band ripple and stop band attenuation. Once these parameters have been loaded, the software determines the filter configuration that will meet the specifications, calculates the FIR coefficients, and gives the results shown at the bottom of the screen. When this operation is complete, it saves the output files and shows the filter characteristics as defined by the parameters in the upper right of this screen.

Deci-mate software is free to qualified customers.

HSP43220 Filter Design Example

HDF Frequency Response

Magnitude (dB): -3.2192, -50.4144, -97.6096, -144.804, -192

Frequency (Hz): 0, 4e+06, 8e+06, 1e+07, 1e+07

FIR Frequency Response

Magnitude (dB): -3.2201, -33.9581, -71.1364, -108.314, -145.493

Frequency (Hz): 0, 1e+04, 2e+04, 3e+04, 5e+04

System Frequency Response

Magnitude (dB): -0.0065, -47.6682, -95.3298, -142.991, -190.653, -238.314

Frequency (Hz): 0, 10000, 20000, 30000, 40000, 50000

206682
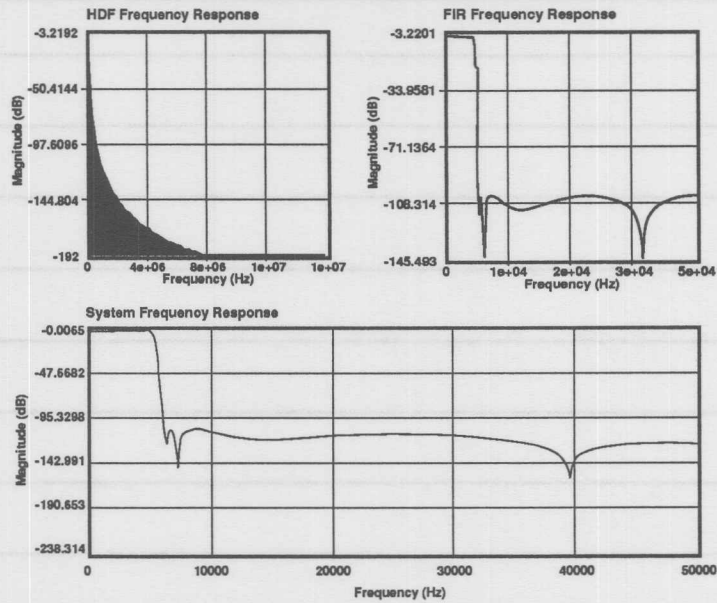
HSP43220 DDF Simulator Specification

DECI•MATE FILTER DESIGN SCREEN

DESIGN MODULE	SIMULATOR MODULE	PROM MODULE

D E C I • M A T E

HSP43220 DDF SIMULATOR SPECIFICATION

Filter file	:	Harris.DAR	
Probe Display	:	HEX	
Save Cont. Output	:	No	Input Rate : **33MHz**
Display Mode	:	CONTINIOUS	Output Rate : **100kHz**

INPUT SIGNAL SPECIFICATION

Signal Origin   :   GENERATED

			Amplitiude	Frequency	Phase
Signal #1	:	COSINE	1.00	5kHz	0.00
Operator	:	NOP			

206683

The frequency response of the Decimating Digital Filter is shown here. In the upper left is the response of the first stage. Notice that it is really a sinc squared function, but due to the scale of this display the lobes have been compressed so that all that is visible is the envelope of the function. In the upper right is the response of the FIR, where the frequency scale goes from 0 to Fs/R. At the bottom is the combined response of the two stages; notice the flatness of the pass band and the attenuation of greater than 96 dB, as specified in the specification screen.
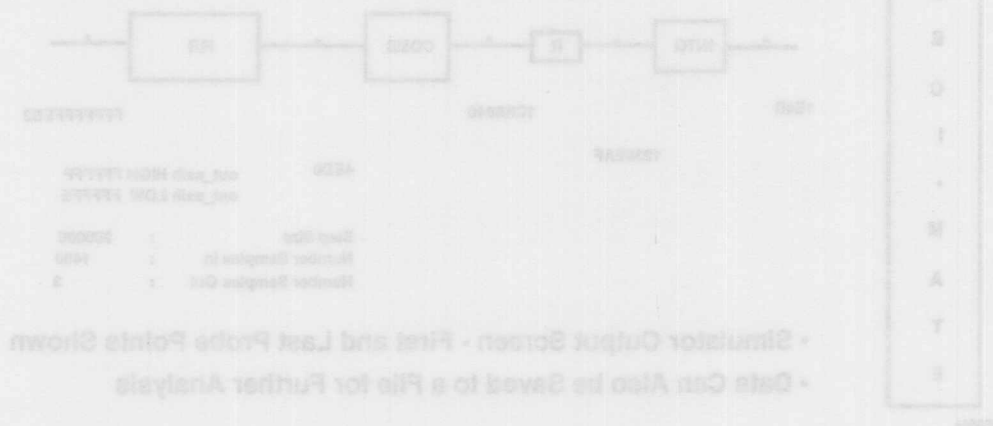
The Deci-mate software also provides a simulator for the DDF. This module takes the configuration previously described and processes it using a model of the actual part. This is a bit true model; that is, it uses the same number of bits in the registers, performs multiplication in the same way and so on.
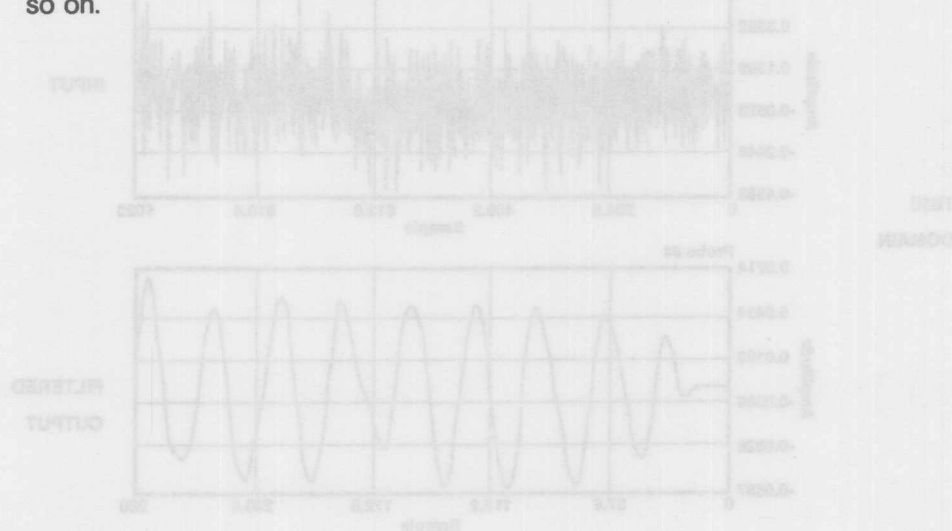
DECI•MATE Simulator

Probe Selector and Monitor

DESIGN MODULE	SIMULATOR MODULE	PROM MODULE

HSP43220 DDF SIMULATOR - MAIN

D
E
C
I
•
M
A
T
E

```
*──[ INTG ]──*──[ R ]──*──[ COMB ]────*────[ FIR ]────*──
```

1E4B   1C6A840   FFFFFFFEB2

    1238EAF

                                    4ED0   out_selh HIGH FFFFFF
                                              out_selh LOW FFFFFE

                                    Step Size   :   200000
                                    Number Samples In :   1400
                                    Number Samples Out :   3

- **Simulator Output Screen - First and Last Probe Points Shown**
- **Data Can Also be Saved to a File for Further Analysis**
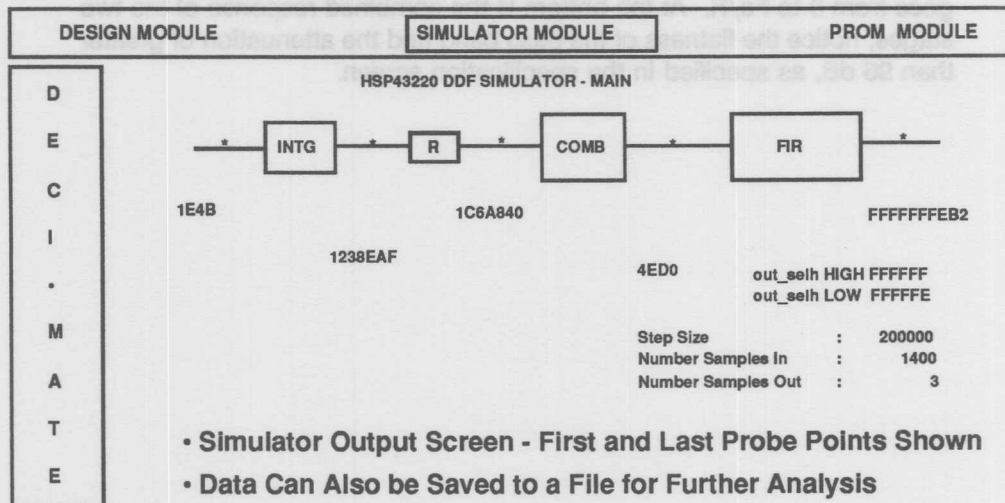
206684

HSP43220 Filter Simulator Example

TIME DOMAIN

Probe #0 — INPUT — Amplitude vs Sample (0 to 1023)

Probe #4 — FILTERED OUTPUT — Amplitude vs Sample (0 to 280)
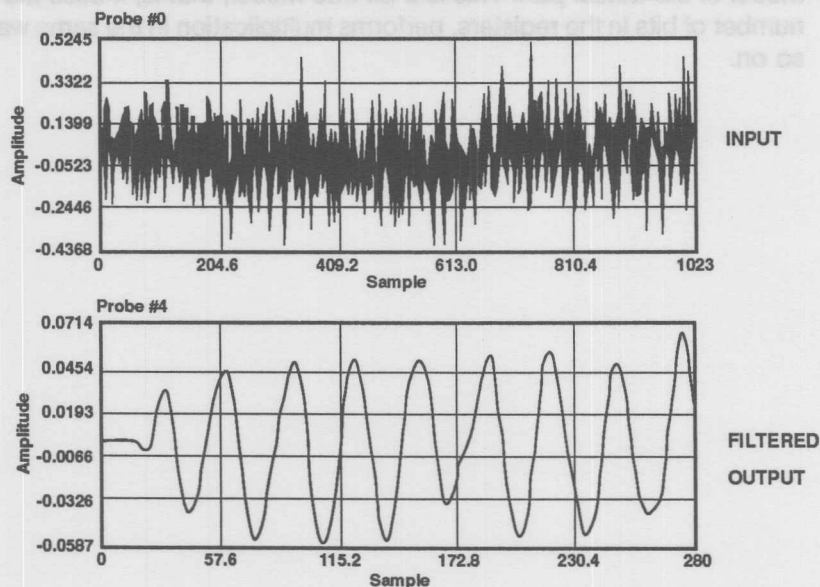
206685

The user can select probes at various points in the model so that the data passing through the part can be monitored. The user can select from various options for input data to the simulator. These options include sine wave, ramp, swept sine wave and random noise; the input data can also be the sum or product of any two of these options; in addition, the user can apply externally generated data to the input.

The output of the simulator can be saved to a file or displayed on the screen one sample at a time while the simulator is running. In this example, the noisy input data has been filtered and decimated as shown.

All I/O files have an easy to use ASCII format so that data can be imported and exported between the simulator and other DSP analysis packages. The formats are given in the back of the Deci-mate manual.

HSP43168 Dual FIR Filter

```
Data ──▶ ┌─────┐ R_O ●──────▶ ┌──────────┐ Real ──────▶  ⎫
Input     │ R_IN│              │ HSP43168 │                ⎬ Wideband
          │     │ I_O ●──────▶ ├──────────┤ Imaginary ──▶  ⎭ Output
          └─────┘              │ HSP43168 │
         HSP45116              ├──────────┤
                               │ HSP43220 │ Real ──────▶  ⎫
                               ├──────────┤                ⎬ Narrowband
                               │ HSP43220 │ Imaginary ──▶  ⎭ Output
                               └──────────┘
```

- Wideband Filter: Decimation by 1 -16
  Narrowband Filter: Decimation by 16 - 16, 384

- For Instrumentation or Spectral Analysis: Search for Signal Using
  Wideband, Switch to Narrowband for Analyzing Individual Signal

206686

45MHz 32 Tap Filter Using HSP43168s

```
Input ──────────────────▶ ┌──────────┐   Even
Data                      │ HSP43168 │   Samples ──▶ Output
                          │ CLK      │              Data
                     ┌──○─┤ OEH      │
                     │    └──────────┘
                     │    ┌──────────┐
                     ├───▶│ HSP43168 │
                     │    │ CLK      │
                     │ ┌○─┤ OEH      │   Odd
                     │ │  └──────────┘   Samples
Data ──────┐  ┌────┐ │ │
Clock      └─▶│  Q ├─┘ │
              │D ──┤   │
              │ ─Q ├───┘
              └────┘
```
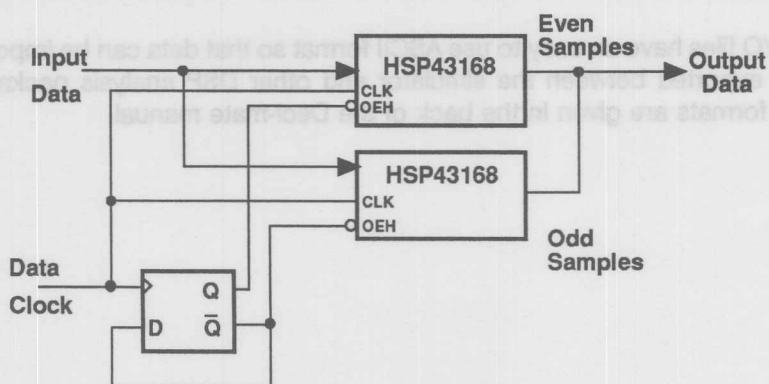
- Both Filters Programmed for 32 Taps, Decimate by 2

206687

The DDF is optimized for filters with high orders of decimation; it achieves its greatest benefit when the decimation factor is 100 or more. In many applications, such as PSK receivers and energy detectors, the user either cannot cope with the pipeline delay of a multitap filter, or needs to process wide band signals.

For the case where the user needs to examine both wide and narrow band signals, the following circuit is presented. Here the NCOM is used as before to shift the frequency of interest to base band. In this example, however, the user can search the spectrum for signals of interest using the HSP43168 as a wide band filter; when a signal of interest is detected, the user selects the output of the DDF's and performs narrow band analysis.

The 43168 can be configured for decimation from 1 to 16. The total number of taps in the filter is the decimation factor times 16; therefore, a filter can be designed with as many as 256 taps.
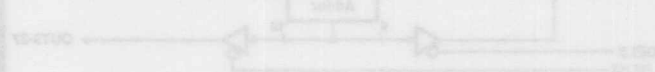
Filters longer than 16 taps can be implemented by using two 43168s, setting each for a decimation by two and toggling between the two outputs on alternate clocks. This can be expanded up to the 43168s coefficient RAM size: 256 coefficients. A 256 tap filter at a 45 MHz data rate would take 16 43168s. This would be a lot of hardware but the user that has this application has a limited number of options.
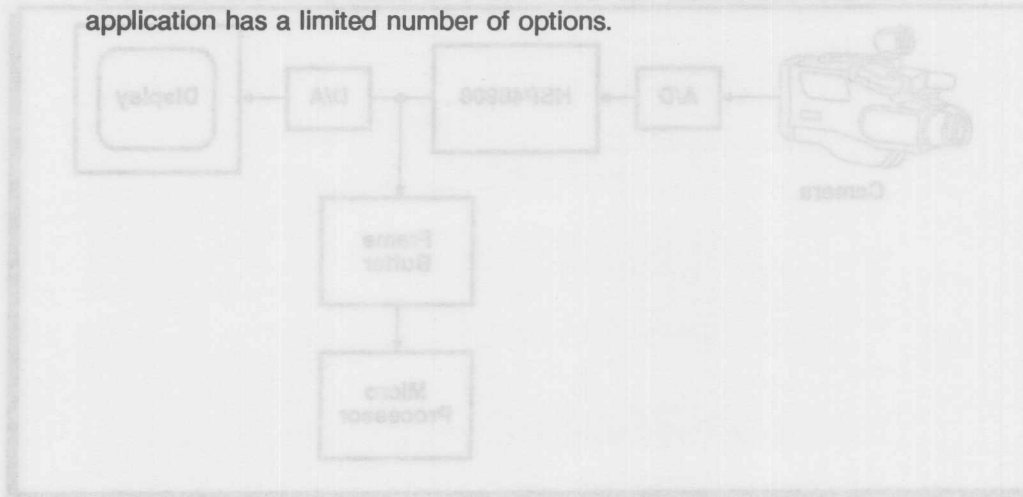
HSP43168 Dual FIR Filter

- **10 BIT DATA, COEFFICIENTS**
- **DECIMATION BY 2-16**
- **SPEED GRADES:**
  - 45, 33MHz Commercial
  - 33, 25.6MHz/883
- **PACKAGING: 84 PGA, PLCC**
- **CONFIGURABLE AS TWO 8-TAP OR ONE 16-TAP FIR FILTER**
- **UP TO 16 X 16 2D FILTERS**
- **ON-CHIP STORAGE FOR 32 COEF/TAP**

CIN0-9 /10
A0-8 /9
WR#

Control/ Configuration

Coefficient Bank A
Coefficient Bank B

INA0-9 /10
FIR A
MUX
FIR B

MUX

INB0-9 /10

MUX/ Adder

OEL#
OEH#
/9
/19
OUT9-27
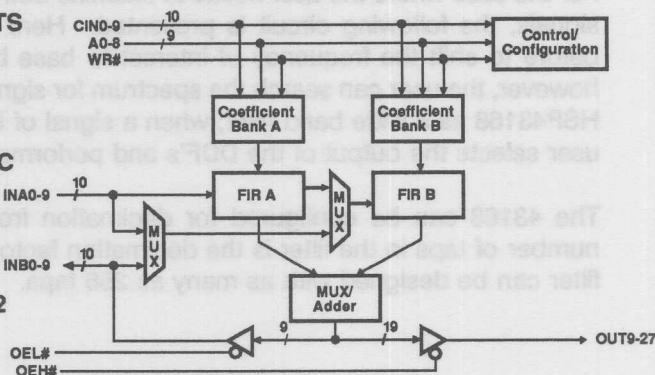
206688

HSP48908 Filtering Images at Video Rates

Camera → A/D → HSP48908 → D/A → Display

Frame Buffer

Micro Processor
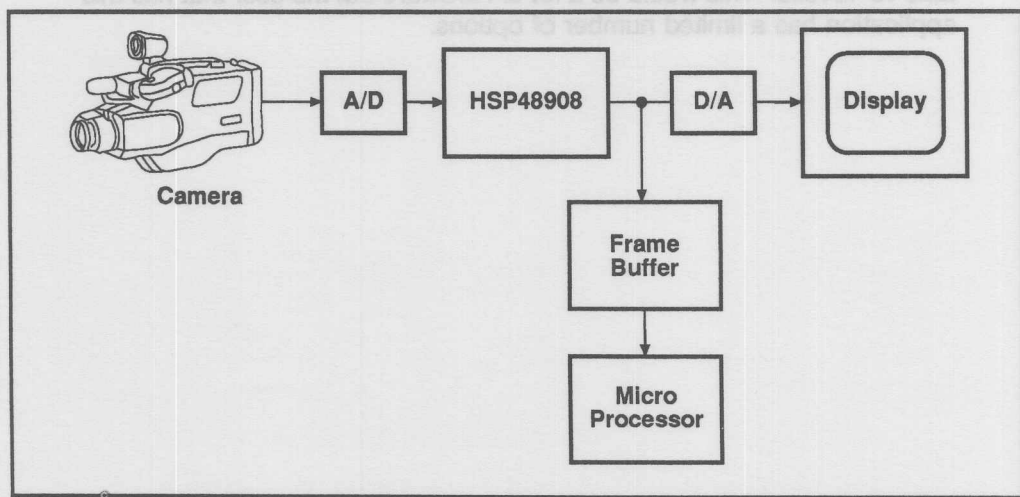
206689

In addition to filtering at high sample rates with low to medium factors of decimation, the HSP43168 can be configured to function in a variety of applications. The HSP43168 processes 10 bit data and coefficients, carries on board storage for 256 coefficients. The coefficients are stored in 32 banks of 8 coefficients each. The 43168 multiplies a set of data samples by the eight coefficients on every clock. The user can select the bank of coefficients to be used during a given clock cycle, which allows for the implementation of adaptive filters.

The FIRs contain four multipliers each, which can be configured to implement two eight tap FIR's or one 16 tap FIR. Furthermore, the mux/adder on the output can be set up to shift and add the outputs of the two filters, so that a single chip can implement a four tap filter with either 10 bits of data with 19 bit coefficients or 19 bit data and 10 bit coefficients. With two chips, one can have a filter with 19 bit data and coefficients.
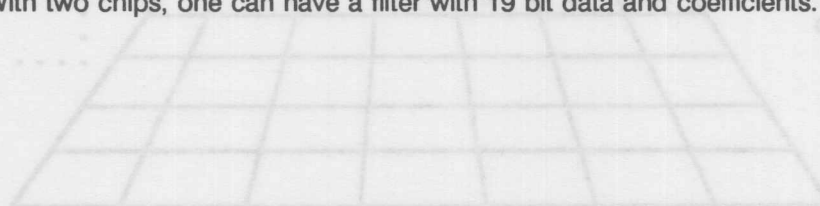
So far we have been talking about processing one dimensional signals; working on two dimensional signals requires a different set of solutions if the requirement is for real time processing. This is an example of a real time image processing system. The HSP48908 Two Dimensional Convolver acts as a filter which can perform a high pass, low pass, edge detection, matched filter, or anything else the user desires. The 32 MHz data rate allows the user to accept data from a camera with no external hardware; with the addition of a FIFO after the A/D, the 2D Convolver can process 1K x 1K images at a 30 Hz frame rate.
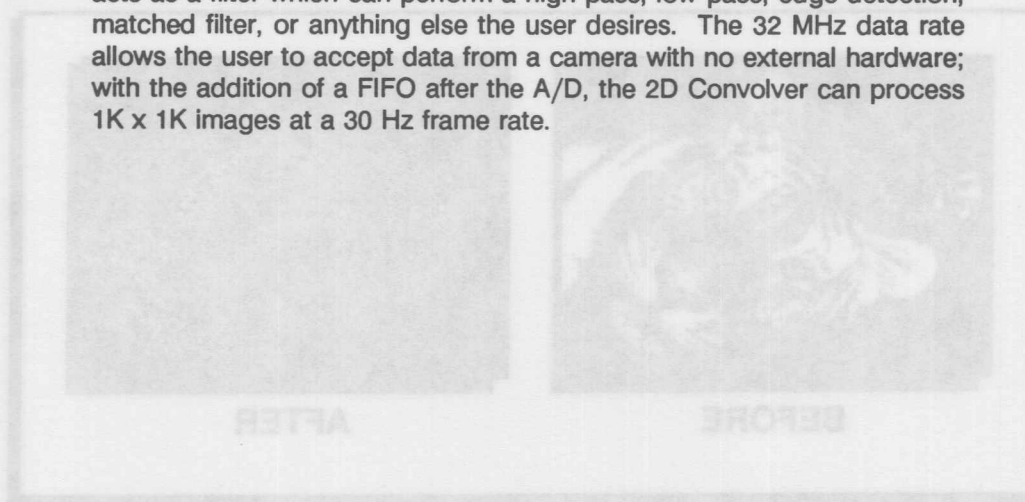
Two Dimensional Convolution

NEW CENTER PIXEL

$$\text{NEW CENTER PIXEL } P_{22} = \sum_{N=1}^{9} P_N \cdot C_N$$

P_{22} EQUALS

3x3 FILTER KERNEL COFFICIENTS

C_1 C_2 C_3
C_4 C_5 C_6
C_7 C_8 C_9

X

3x3 ARRAY OF PIXELS

IMAGE PIXELS

P_{11} P_{12} P_{13} P_{14} P_{15} P_{16} ROW 1
P_{21} P_{22} P_{23} P_{24} P_{25} ROW 2
P_{31} P_{32} P_{33} P_{34}
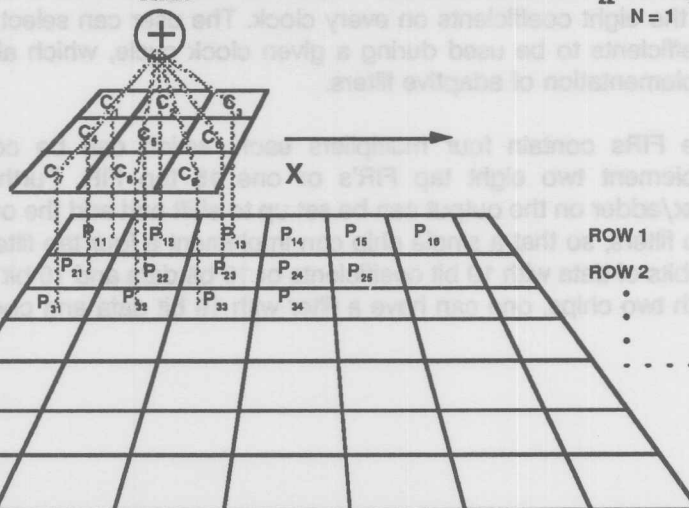
206689A

Edge Detection

BEFORE   AFTER

206689B

104
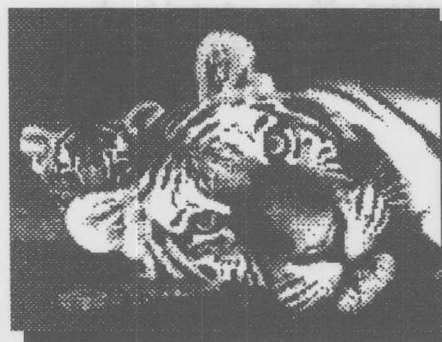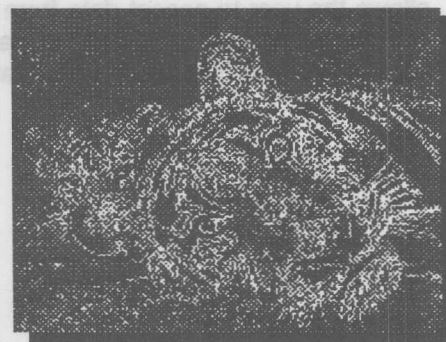
Two dimensional convolution is the process of multiplying the elements of a kernel by the corresponding image pixels, adding the products and storing the result in an output image. The kernel is then moved over one pixel and the process is repeated. At the end of the row, the kernel is placed at the beginning of the next row and the process continues as before.

This example shows a 3 x 3 convolution.
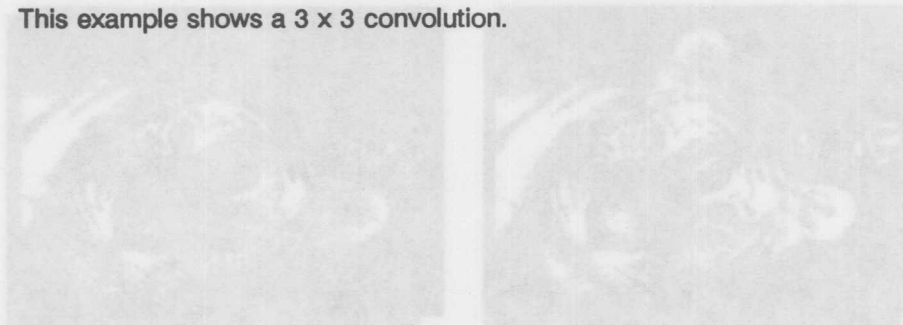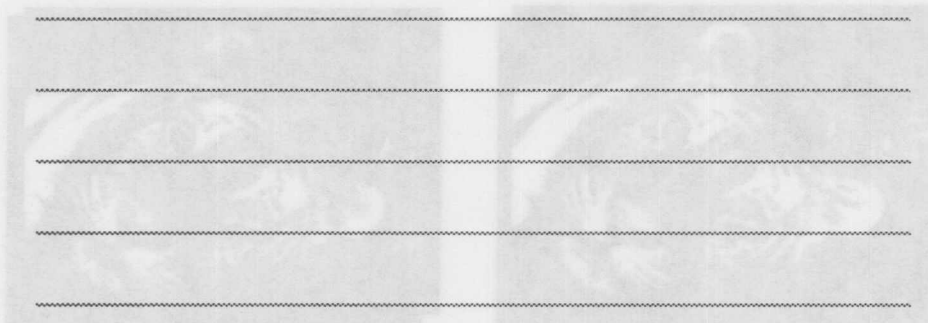
High-Pass Filtering
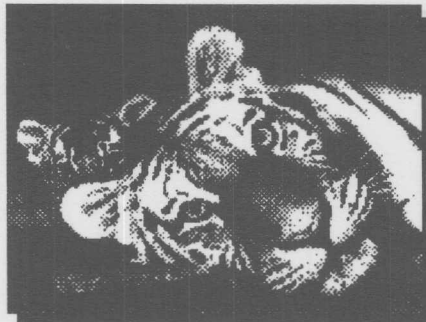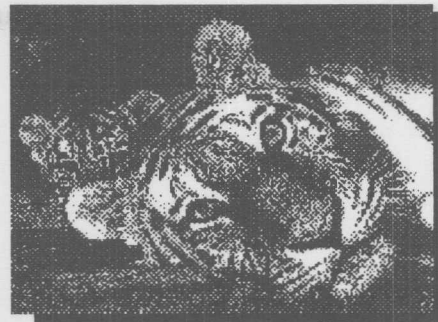
BEFORE   AFTER

206689C

Low-Pass Filtering
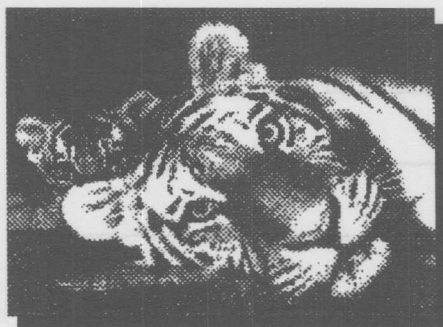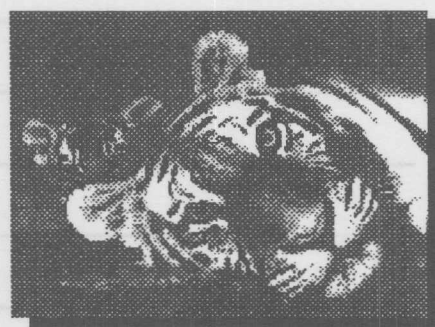
BEFORE   AFTER
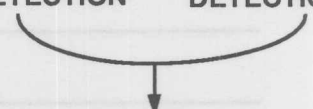
206689D
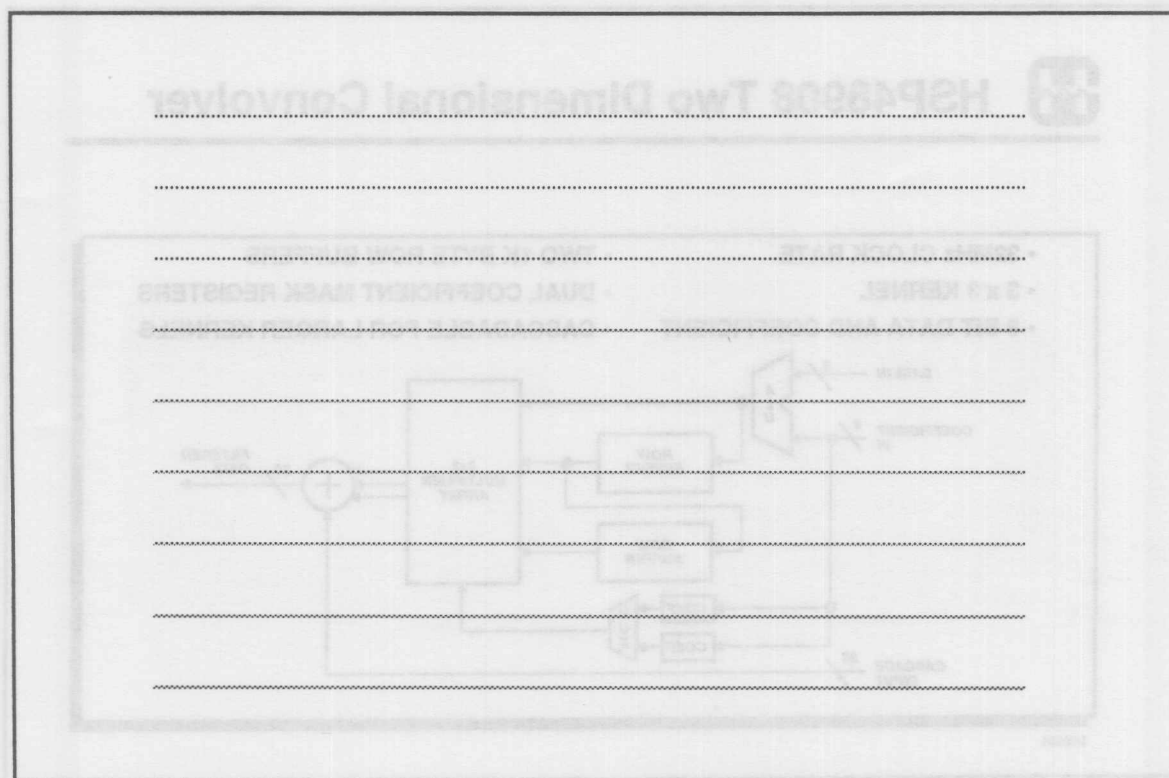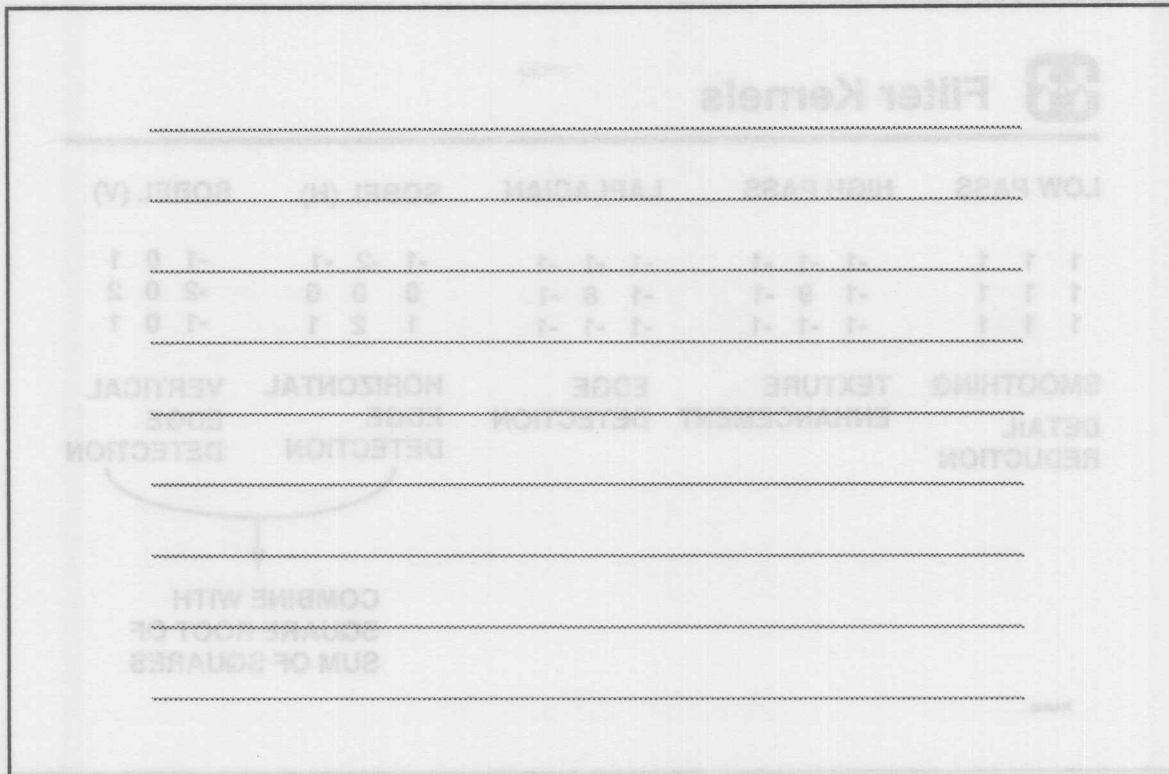
Filter Kernels

LOW PASS	HIGH PASS	LAPLACIAN	SOBEL (H)	SOBEL (V)
1 1 1	-1 -1 -1	-1 -1 -1	-1 -2 -1	-1 0 1
1 1 1	-1 9 -1	-1 8 -1	0 0 0	-2 0 2
1 1 1	-1 -1 -1	-1 -1 -1	1 2 1	-1 0 1
SMOOTHING DETAIL REDUCTION	TEXTURE ENHANCEMENT	EDGE DETECTION	HORIZONTAL EDGE DETECTION	VERTICAL EDGE DETECTION

COMBINE WITH
SQUARE ROOT OF
SUM OF SQUARES

206689E

HSP48908 Two Dimensional Convolver

- 32MHz CLOCK RATE
- 3 x 3 KERNEL
- 8 BIT DATA AND COEFFICIENT
- TWO 1K BYTE ROW BUFFERS
- DUAL COEFFICIENT MASK REGISTERS
- CASCADABLE FOR LARGER KERNELS

206691

108

When filtering images, a specialized filter architecture is needed if real time processing is required. In this case, the information from three consecutive rows of the image must be available simultaneously. The HSP48908 solves this problem by including two on board row buffers, each 1024 bytes long. The length of these buffers is programmable, so an image of any width, from 3 pixels to 1024 can be processed. The input information, plus the output of the row buffers, is multiplied by the filter coefficients in a 3 by 3 array of 8 bit multipliers. There are two sets of registers to store the coefficients; this allows the user to download a new coefficient kernel during operation.
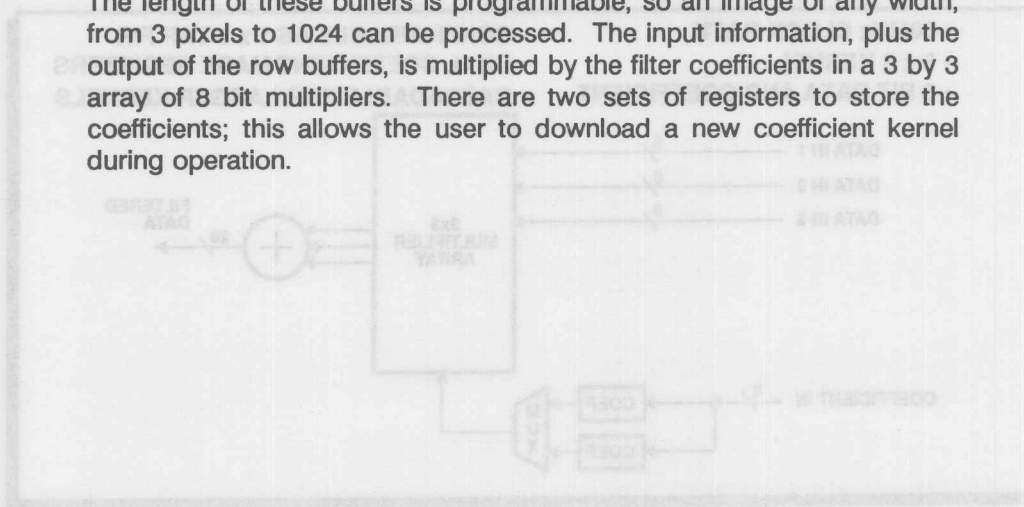
Choosing Output Bit Range

MOST APPLICATIONS:

- All Kernal Coefficients are Known
- Set Ouput Bits According to Gain in Filter

Gain in kernal = Σ Cij, Cij = coeffient values

Data 8 → D_{IN} 0-7 D_{out} 19 → N →

Coef 8 → C_{IN} 0-7 D_{out} 0

N ≤ 20

HSP48908
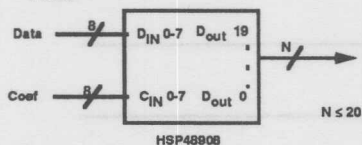
Shift	Output Bits
>1	N bit range starting at $\log_2 \Sigma Cij$
0	Choose Bits so that Desired Resolution is Maintained for Largest Expected Edge (Edge Detectors)

GENERAL CASE:

$\frac{1}{Gain}$

D_{out} 15 : D_{out} 0 16 → X → N →

HSP48908   HMU17

206692

Logic → Overflow
→ Underflow
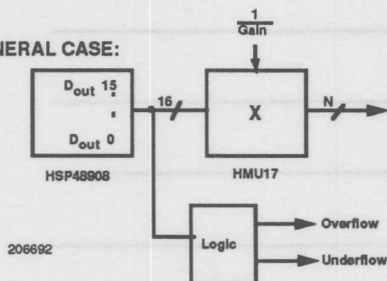
- Compensate for Gain With a Multiplier
- Logic Takes Care of Numbers Greater than Desired Output Range (Overflow) and Negative Numbers (Underflow)

HSP48901 Image Filter

- 30MHz CLOCK RATE
- 3 x 3 KERNEL
- 8 BIT DATA AND COEFFICIENT
- CONFIGURABLE AS 1 x 9 TAP FIR
- DUAL COEFFICIENT MASK REGISTERS
- CASCADABLE FOR LARGER KERNELS

DATA IN 1 ——— 8 →
DATA IN 2 ——— 8 →
DATA IN 3 ——— 8 →

3x3 MULTIPLIER ARRAY → (+) 20 → FILTERED DATA

COEFFICIENT IN — 8 → COEF → M U X
COEF

206693
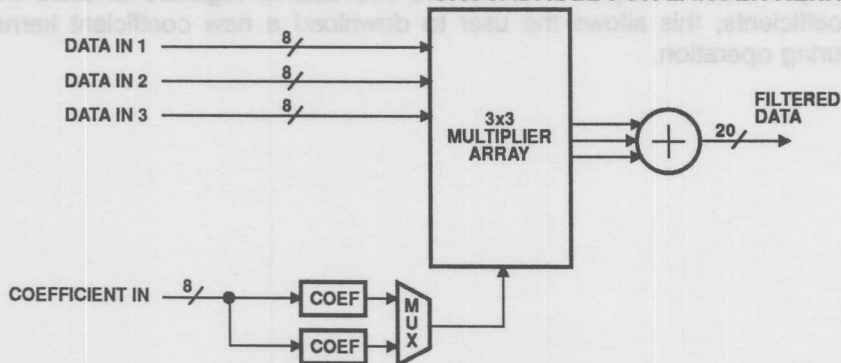
Filters (kernels) with positive and negative coefficients, such as edge detectors, have overflow whose magnitude is dependent on the magnitude of the edge they encounter. In this case, the output bit range should be set so that the bits selected cover the magnitude of the edges that would most likely be detected or would be of maximum interest to the observer.

For images wider than 1024 pixels, the row buffers on the HSP48908 serve no purpose. For those applications, Harris provides the HSP48901 which performs the same function but uses external row buffers. It still uses eight bit arithmetic and has the same dual coefficient registers.
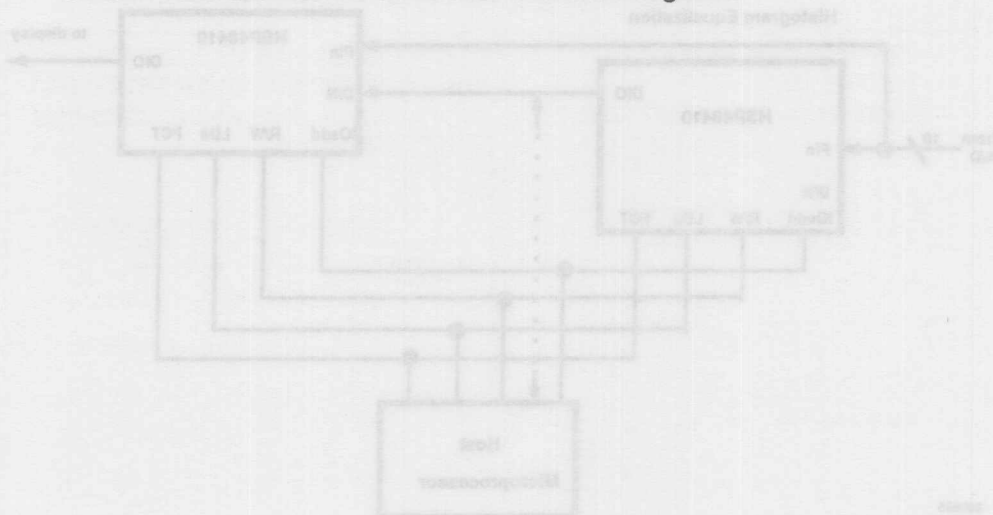
3 X 3 Convolution with HSP48901

IMAGE DATA → 8 → DIN1

HSP9501 BUFFER → DIN2

HSP9501 BUFFER → DIN3

SYSTEM CLOCK → CLK

HSP48901

D_{OUT}0-19 → 20 → FILTERED IMAGE DATA
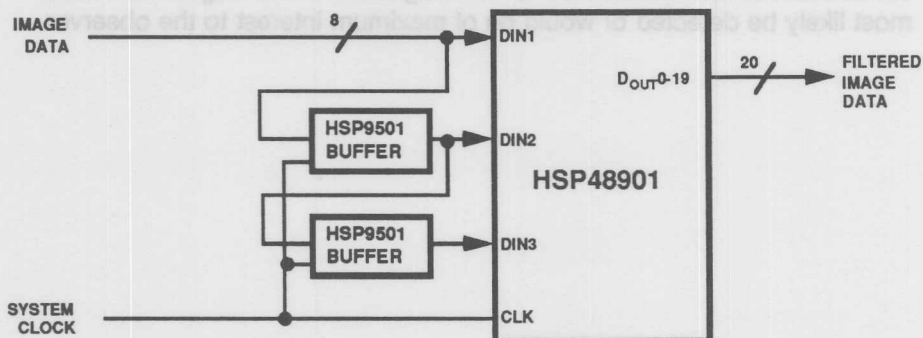
- LOW COST ALTERNATIVE TO HSP48908
- REAL TIME SOLUTION FOR LOW END APPLICATIONS

206694

HSP48410 Real Time Contrast Enhancement

Histogram Equalization

Look Up Table

from A/D → 10 → Pin

HSP48410

DIN

IOadd R/W LD# FCT

DIO

HSP48410

Pin   DIO → to display
DIN
IOadd R/W LD# FCT

Host Microprocessor

206695

112

![Harris Semiconductor logo](HARRIS SEMICONDUCTOR)
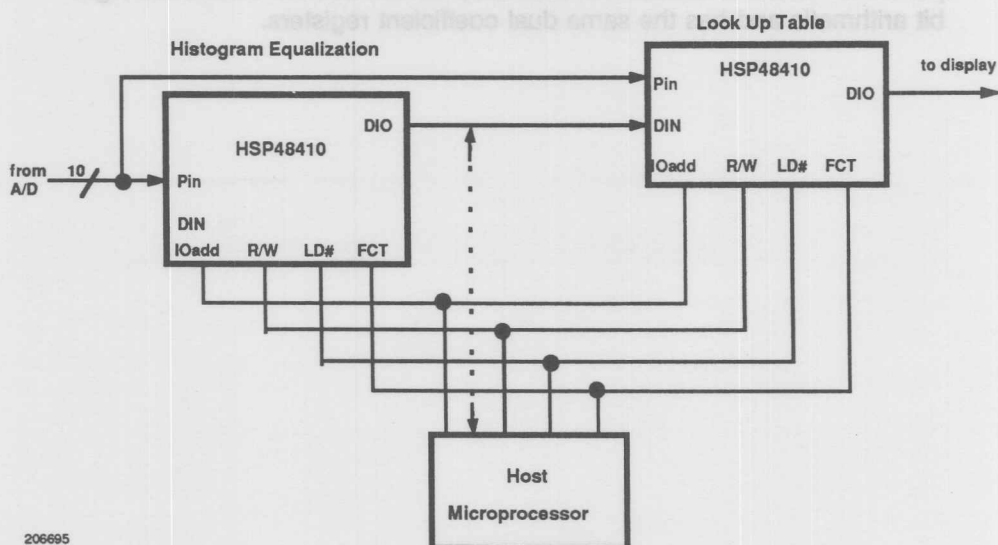
The HSP9501 can be used with the HSP48901 for images up to 1281 pixels wide. When these chips are connected in this manner, the circuit implements the same function as the 2D Convolver. Several HSP9501s can be cascaded end to end for arbitrarily wide images.
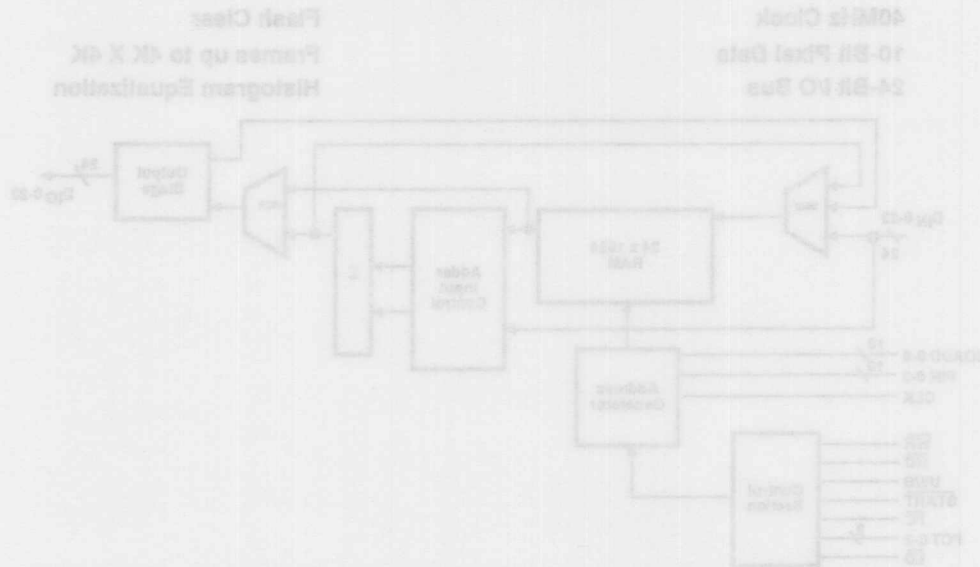
When image contrast is lower than desirable, the HSP48410 can be used to brighten things up. The 48410 has 7 modes, three of which are used in this application. In this block diagram, the first Histogrammer is used to calculate the histogram of an image. When this operation is complete, the part is reconfigured by the host to perform the histogram accumulation; it takes the Probability Density Function computed in the first pass and converts it into the Cumulative Density Function. For a generalized image, this is the optimal transfer function to enhance the contrast.

While this operation is going on, the CDF is passed to the second Histogrammer over a special synchronous interface. The second histogrammer is configured to act as a look up table. Once the data has been downloaded, the image data is passed through the look up table for contrast enhancement, while the first Histogrammer is reconfigured by the host to go back to computing the histogram of the input data. This can be a real time operation if the downloading of the look up table data is done during the video blanking period.

HSP48410 Histogrammer

FEATURES

40MHz Clock

10-Bit Pixel Data

24-Bit I/O Bus

Flash Clear

Frames up to 4K X 4K

Histogram Equalization
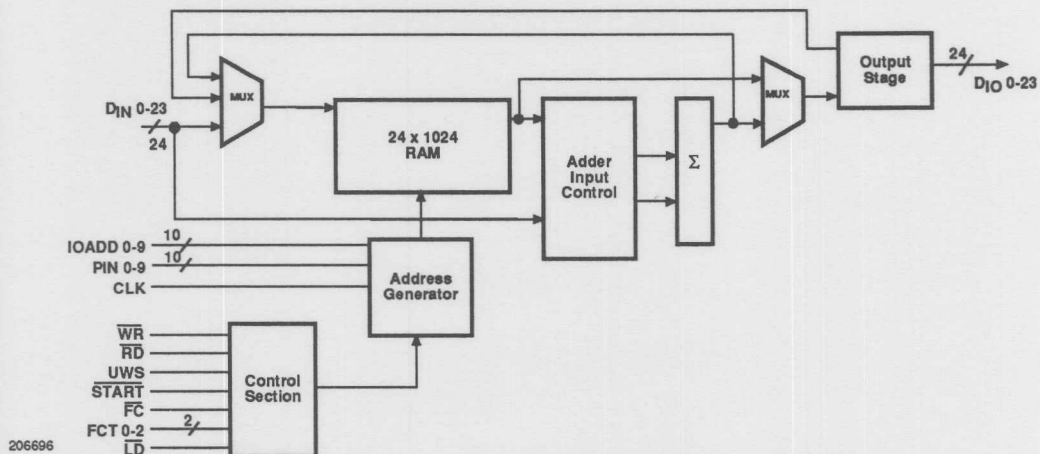
206696

Unequalized Histogram
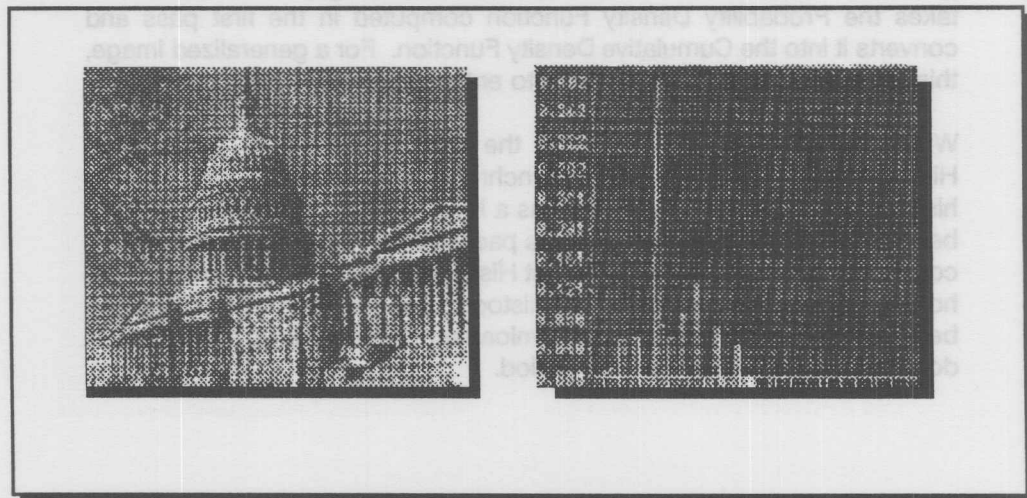
206696A

The HSP48410 consists of a 1024 x 24 bit RAM with the associated arithmetic and control logic needed to perform histogramming, and histogram accumulation. In addition, it can also function as a look up table, row buffer, bin accumulator, or as a delay line with subtract. The configuration of the RAM allows the calculation of a histogram on a 10 bit, 4096 x 4096 image with no overflow. It contains a flash clear and an asynchronous RAM interface for easy interface to a microprocessor.

Equalized Histogram
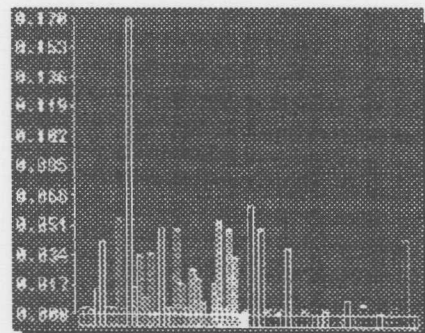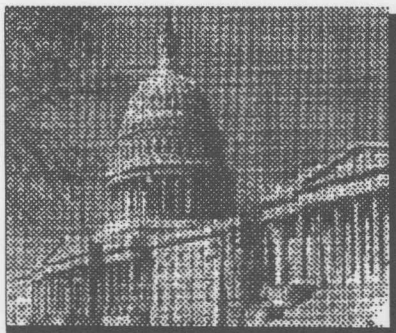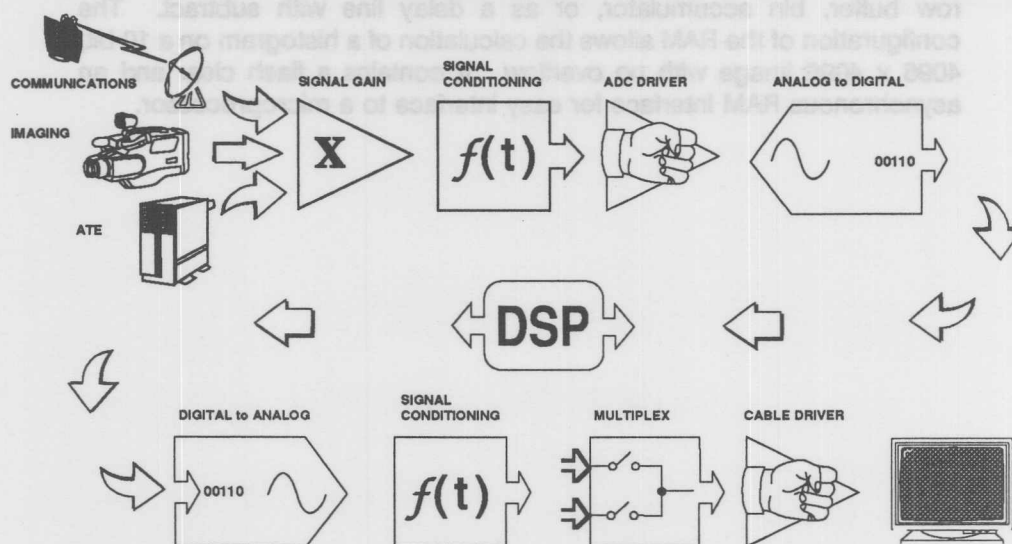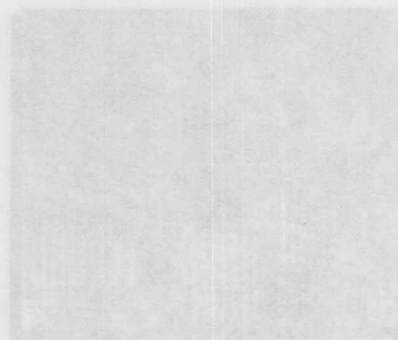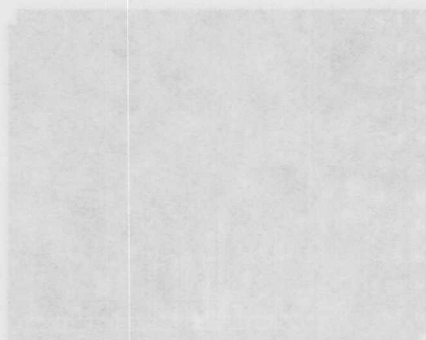
206689B

Video / Imaging Demonstration

COMMUNICATIONS

IMAGING

ATE

SIGNAL GAIN

X

SIGNAL CONDITIONING

$f(t)$

ADC DRIVER

ANALOG to DIGITAL

00110

DSP

DIGITAL to ANALOG

00110

SIGNAL CONDITIONING

$f(t)$

MULTIPLEX

CABLE DRIVER

206697

HARRIS
SEMICONDUCTOR

Image Processing Demonstration System

- PERFORMS REAL TIME VIDEO IMAGE FILTERING
- NO FRAME STORAGE NECESSARY
- PROCESSES 30 FULL FRAMES PER SECOND
- VGA COMPATIBLE OUTPUT

Image Processing Demonstration System

Applications

- MEDICAL IMAGING
- MACHINE VISION
- INSPECTION SYSTEMS
- SECURITY SYSTEMS
- SATELLITE IMAGING
- SPECIAL EFFECTS

HARRIS
SEMICONDUCTOR

Image Processing Demonstration System

- PERFORMS REAL TIME VIDEO IMAGE FILTERING
- NO FRAME STORAGE NECESSARY
- OPERATES ON DOUBLE SPEED NON-INTERLACED SCAN
- PROCESSES 60 FULL FRAMES PER SECOND
- VGA COMPATIBLE OUTPUT

206698

Image Processing Demonstration System

Applications

- MEDICAL IMAGING
- MACHINE VISION
- INSPECTION SYSTEMS
- TARGET ACQUISITION
- SECURITY SYSTEMS
- SATELLITE IMAGING
- SPECIAL EFFECTS

206699
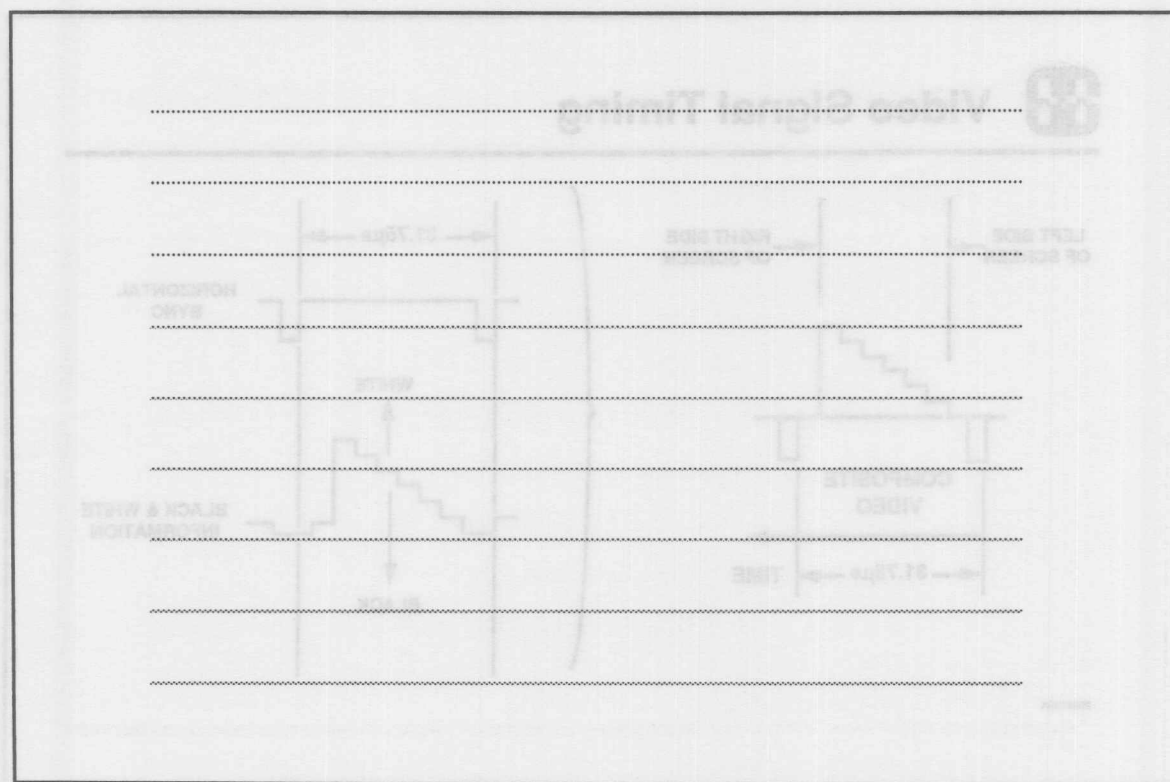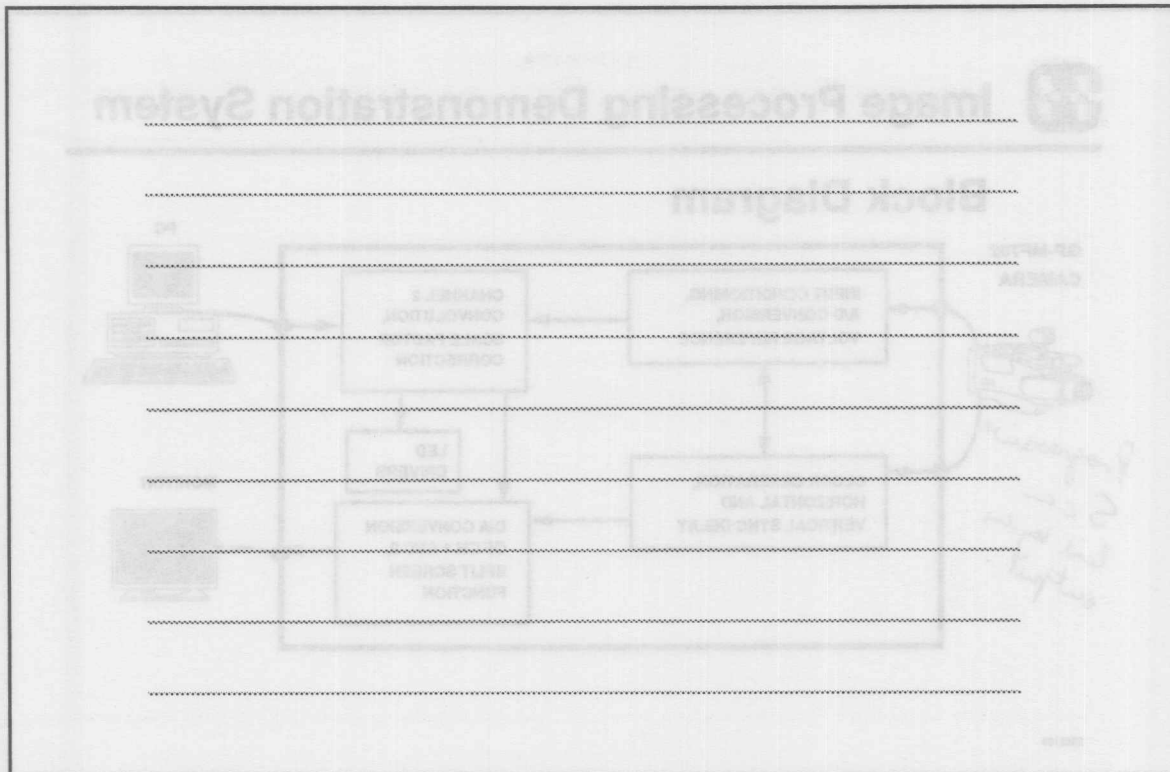
Image Processing Demonstration System

Block Diagram

GP-MF702
CAMERA

*Progressive
Scan.
lin ky lue
output.*

PC

| INPUT CONDITIONING, A/D CONVERSION, VOLTAGE REFERENCE |
| CHANNEL 2 CONVOLUTION, SCALE FACTOR CORRECTION |
| LED DRIVERS |
| CLOCK GENERATION, HORIZONTAL AND VERTICAL SYNC DELAY |
| D/A CONVERSION OF CH 1 AND 2, SPLIT SCREEN FUNCTION |

MONITOR
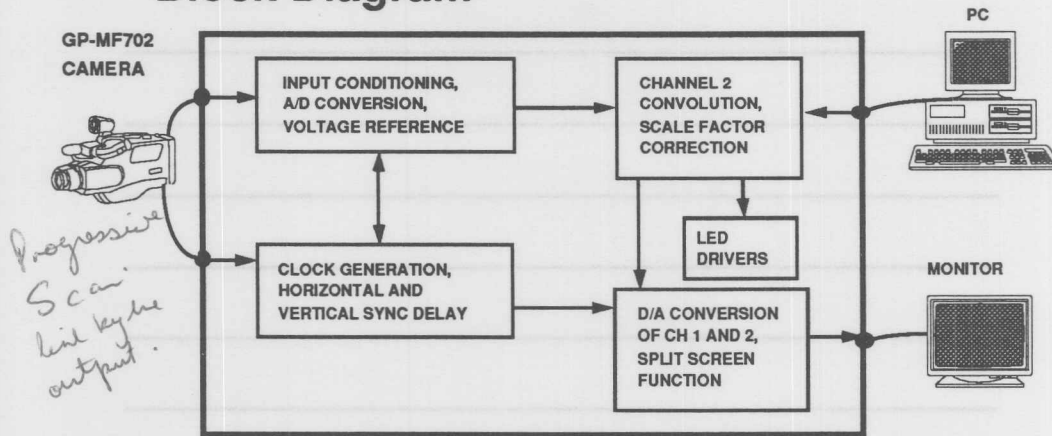
2066100

Video Signal Timing

LEFT SIDE OF SCREEN

RIGHT SIDE OF SCREEN

COMPOSITE VIDEO

31.75μs TIME

31.75μs

HORIZONTAL SYNC

WHITE

BLACK & WHITE INFORMATION

BLACK
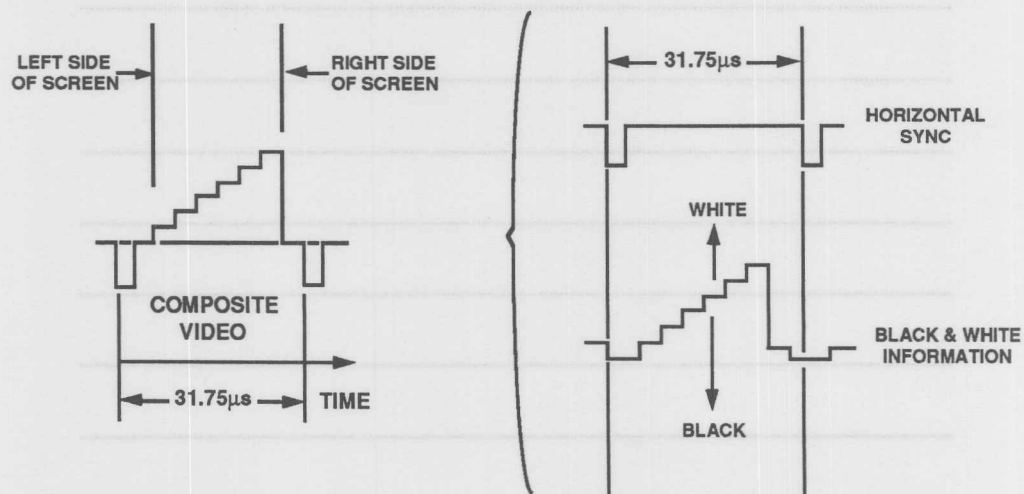
2066100A

Image Processing Demonstration System

Clock Speed Calculation

- FRAME RATE = 60/SECOND (16.67ms/FRAME)

- PIXEL RESOLUTION = 649 (H) x 490 (V)

- HORIZONTAL LINES = 490 DISPLAYED +35 BLANKED = 525

- LINE PERIOD = 16.67ms/525 LINES = 31.75μs

- HORIZONTAL BLANKING INTERVAL = 5.79μs

- PIXEL PERIOD = (31.75μs - 5.79μs) /649= 40ns

- CLOCK SPEED = 1/40ns = 25MHz

2066101

Image Processing Demonstration System
Input Conditioning
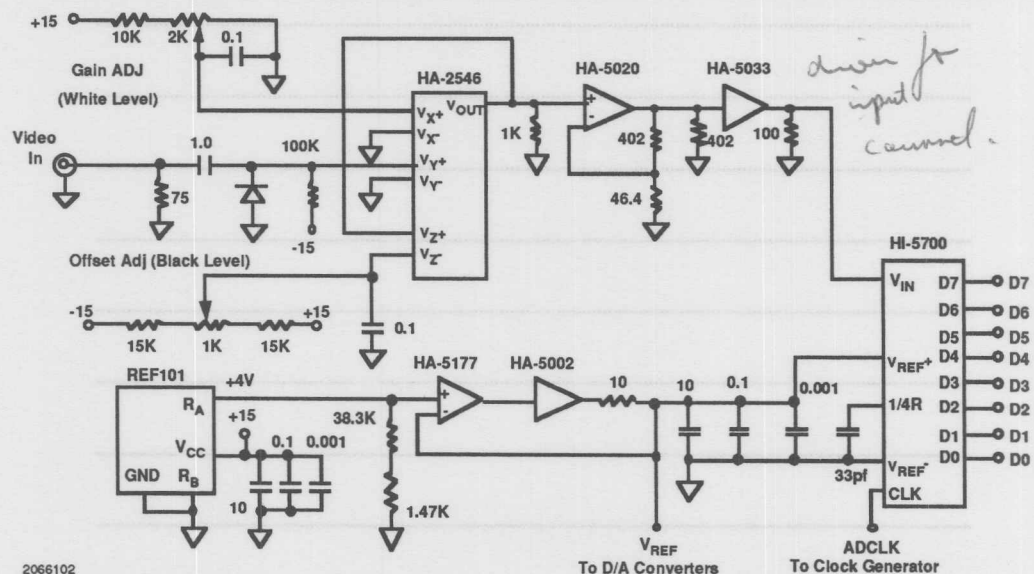
2066102

Image Processing Demonstration System
Clock Generator

Image Processing Demonstration System
Contrast/Brightness/Scale Factor Correction

Image Processing Demonstration System
Clock Generator
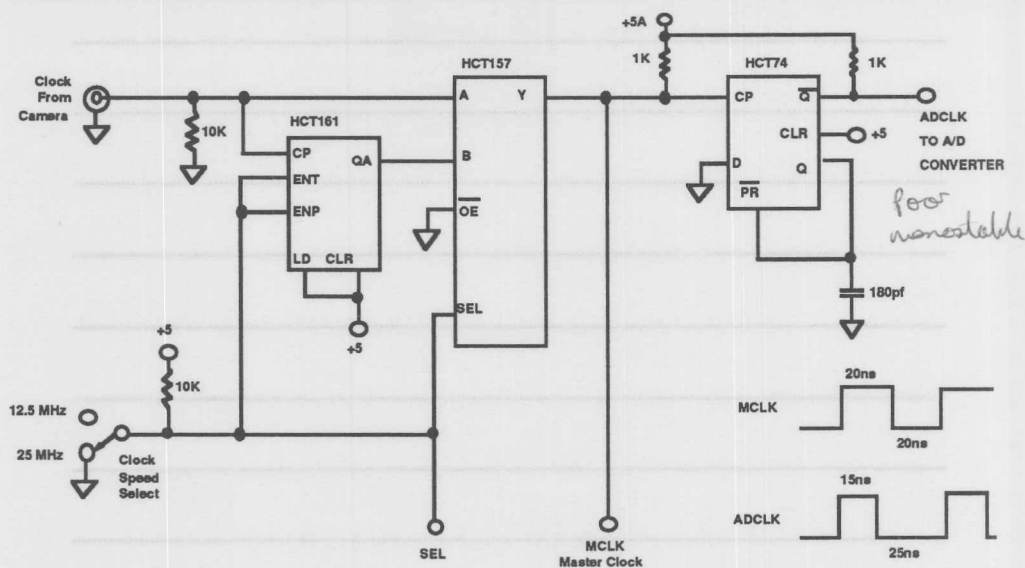
Image Processing Demonstration System
Convolution/Scale Factor Correction
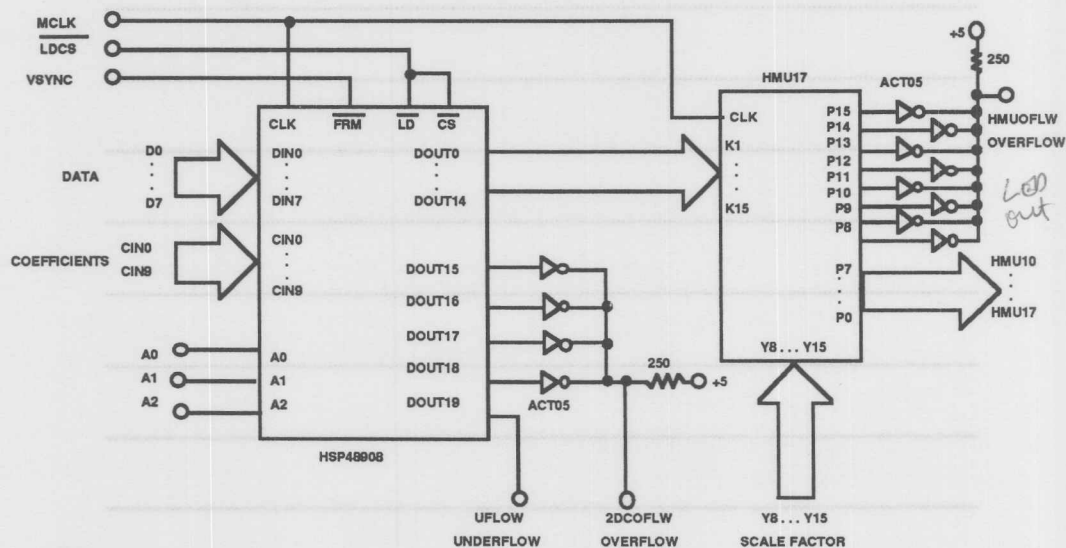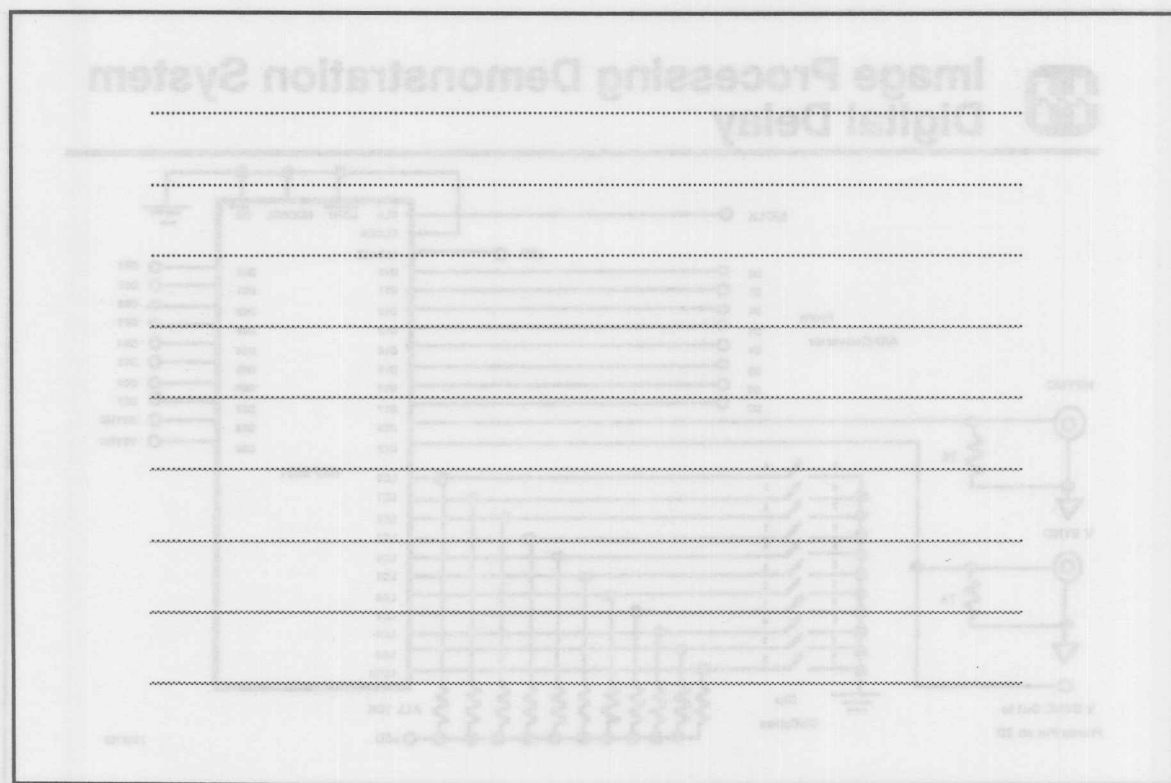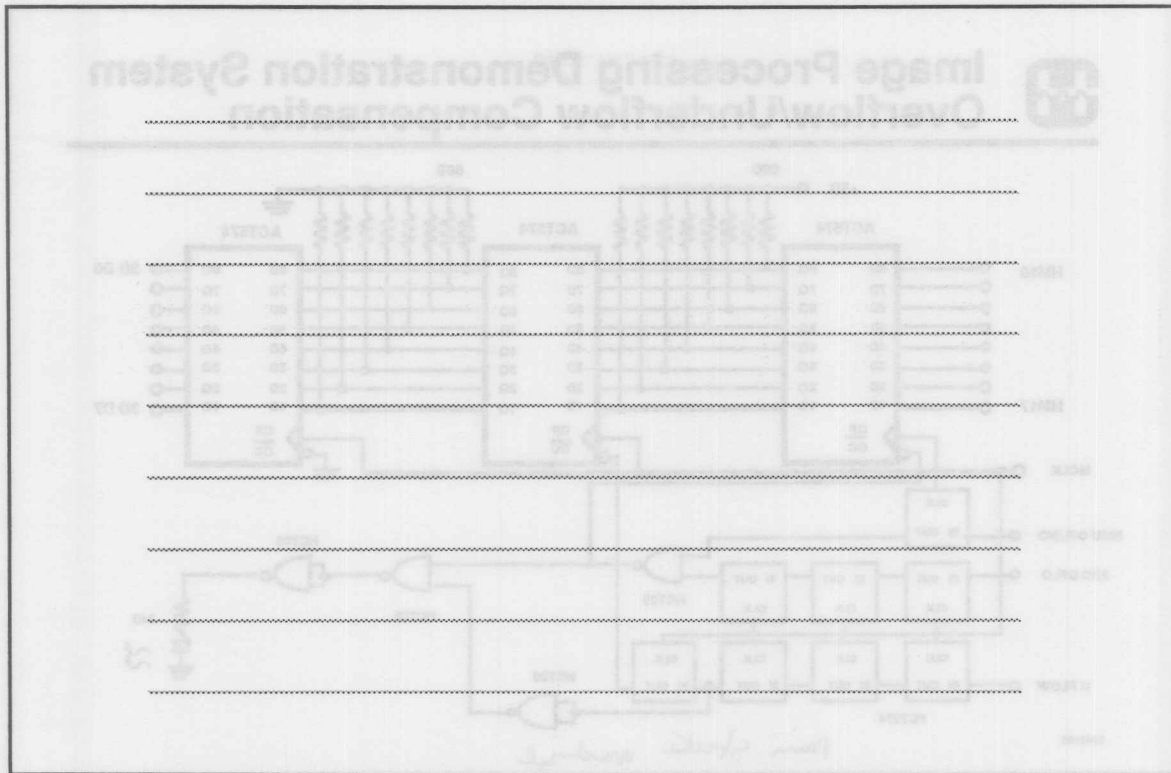
Image Processing Demonstration System
Overflow/Underflow Compensation
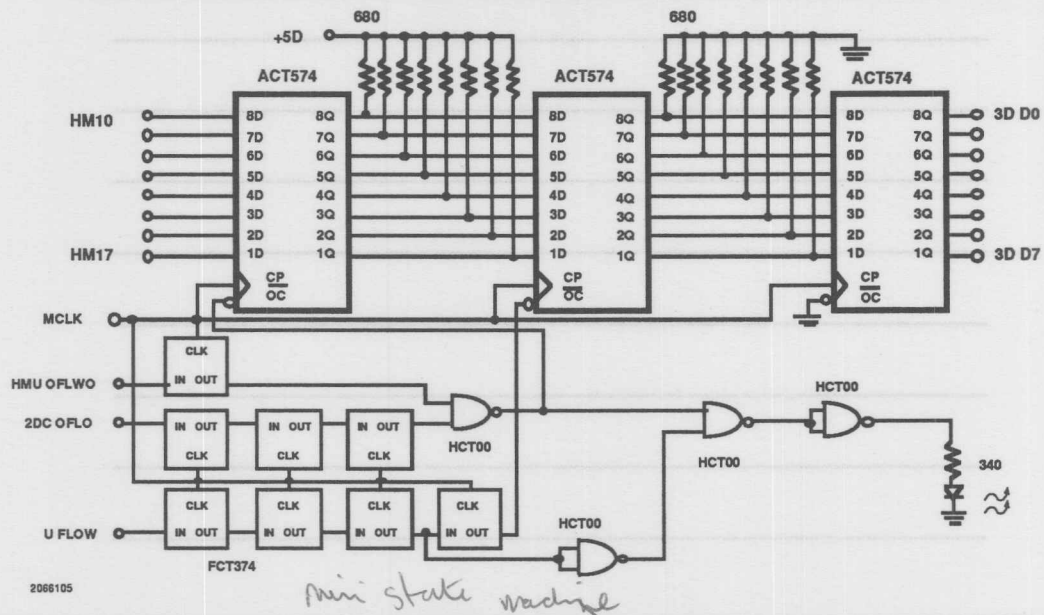
Image Processing Demonstration System
Digital Delay

Image Processing Demonstration System
Overflow/Underflow Compensation

2066105

Image Processing Demonstration System
Digital Delay

2066106
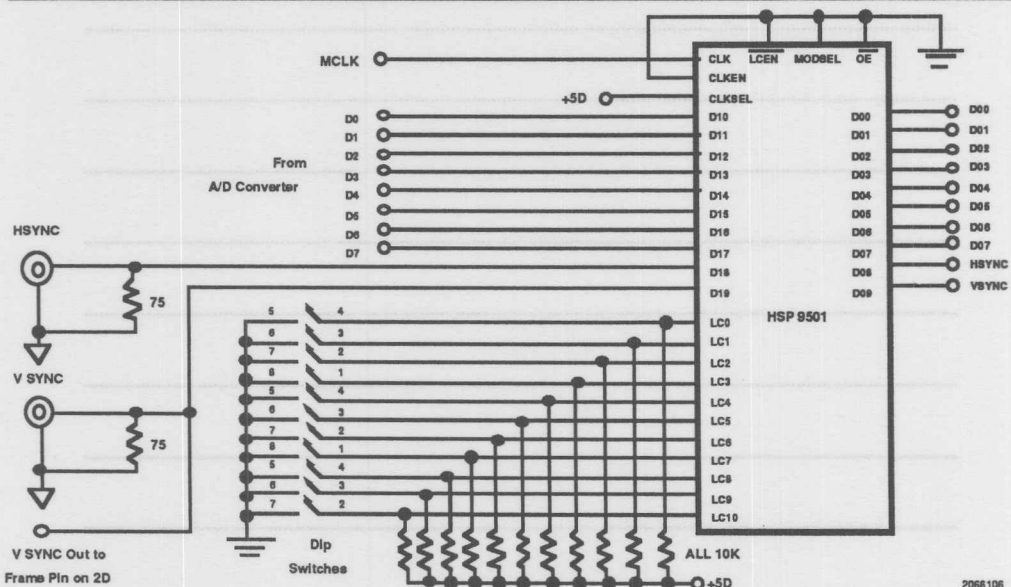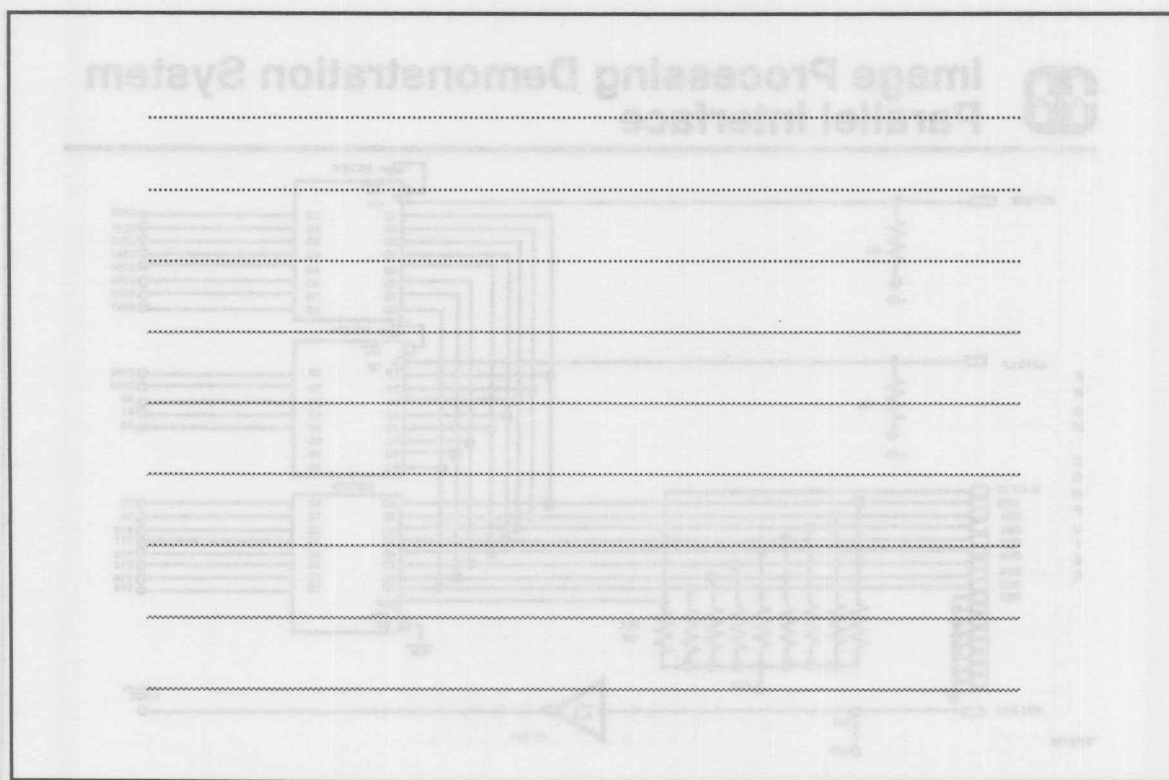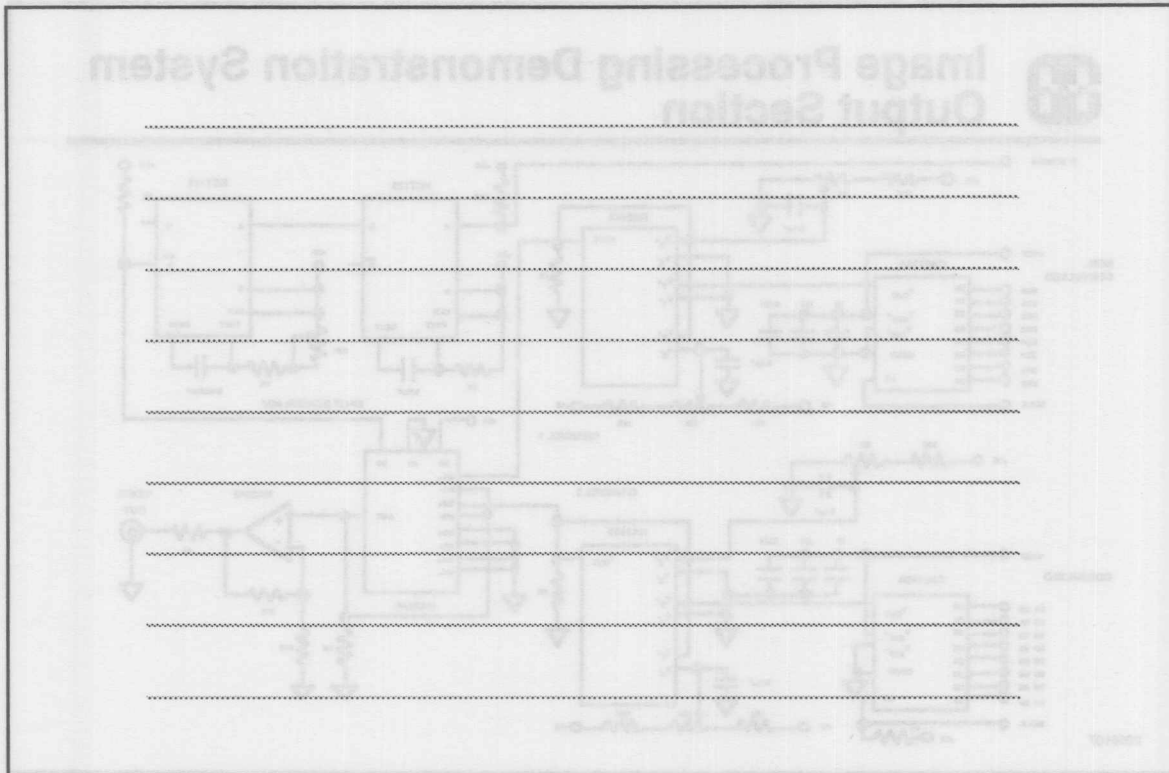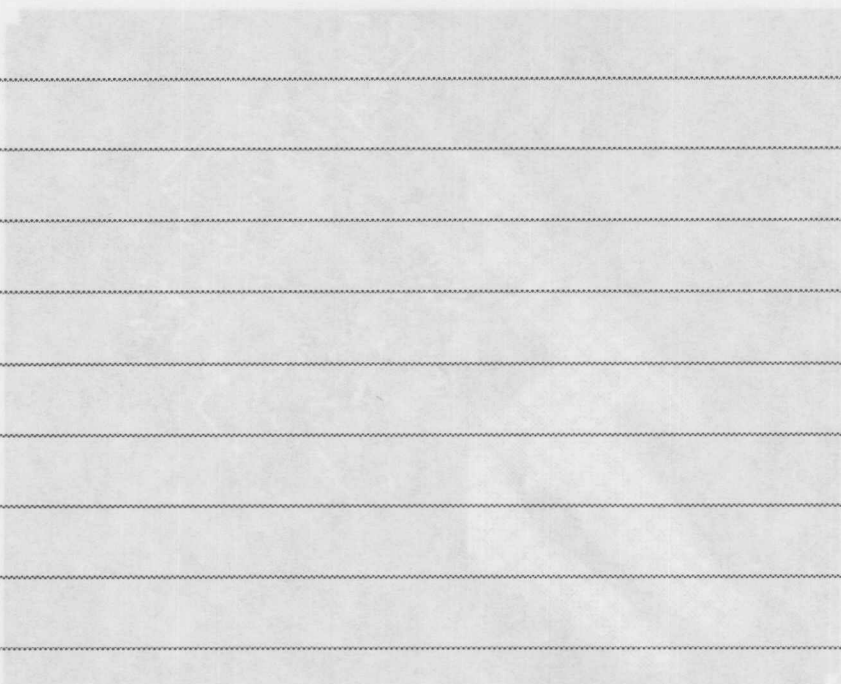
Image Processing Demonstration System Output Section

2066107
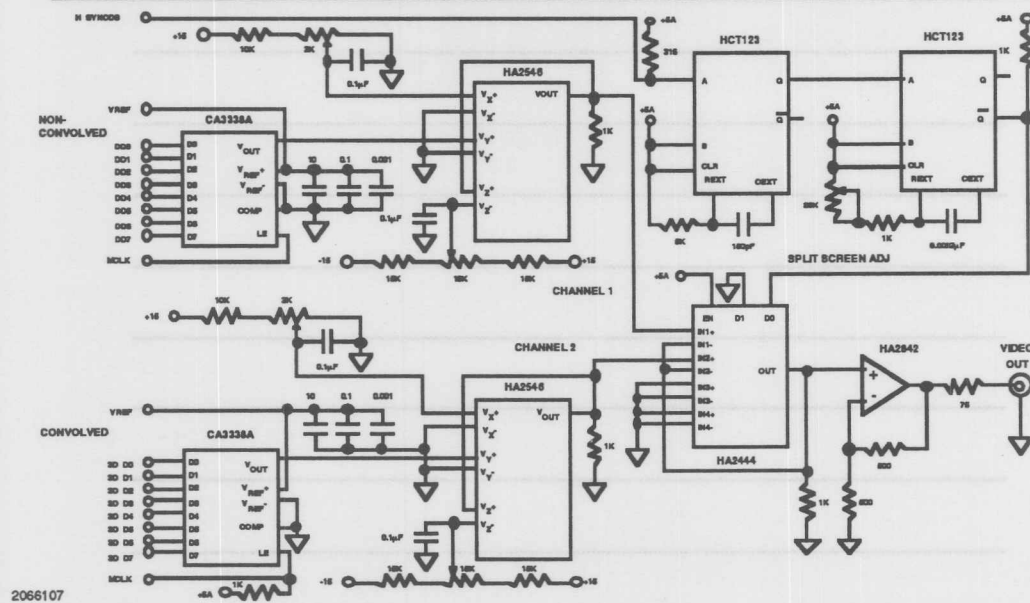
Image Processing Demonstration System Parallel Interface
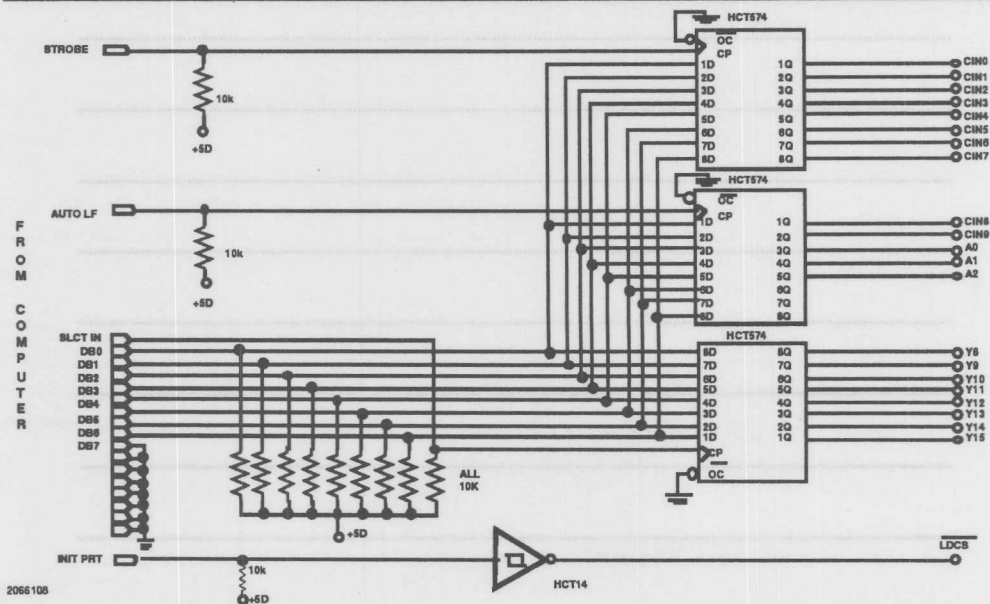
2066108

2066108A

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |

PARALLEL INTERFACE
PAGE 8

PC

CAMERA

GAIN/OFFSET ADJUST, A TO D CONVERSION, TIMING/ VOLTAGE REF
PAGE 2

CHANNEL 2 CONVOLUTION
PAGES 3/4

LED DRIVERS
PAGE 7

CHANNEL 1, H/V SYNC DELAY
PAGE 6

D TO A CONVERSION OF CHANNELS 1 AND 2, ATTENUATION AND SPLIT SCREEN FUNCTION
PAGE 5

MTV!
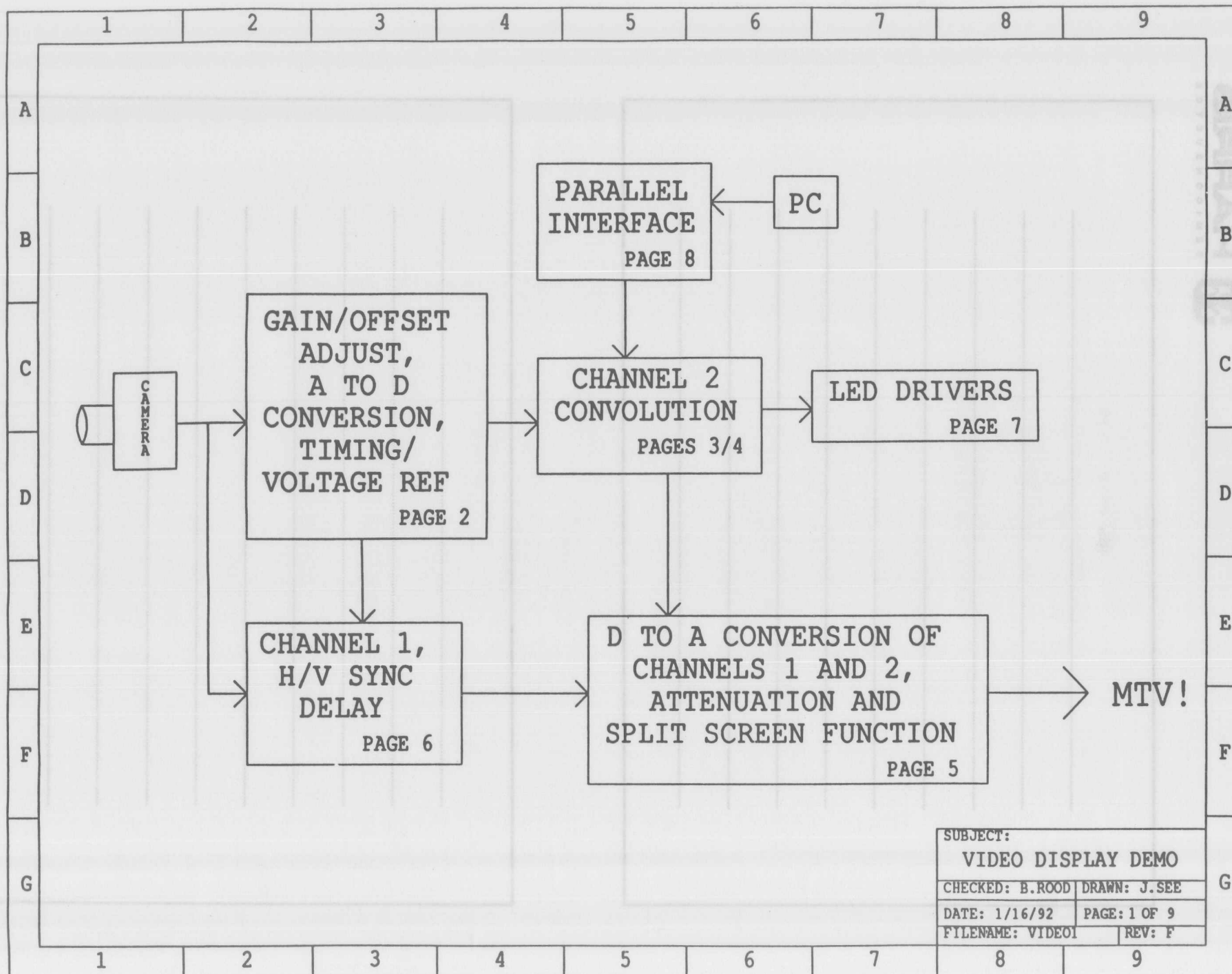
SUBJECT: VIDEO DISPLAY DEMO	
CHECKED: B.ROOD	DRAWN: J.SEE
DATE: 1/16/92	PAGE: 1 OF 9
FILENAME: VIDEO1	REV: F

VIDEO DISPLAY DEMO

+15 R9 10k R59 2K C7 .1uF

VIDEO_IN BNC1 C142 1uF R10 75 D1 1N914 R72 100K -15

HA2546 U1
13 VX+ VOUT 8
12 VX-
9 VY+ GAA 16
VY- GAB 14
GAC 15
10 VZ+
VZ- VYIOA 4
2 VREF VYIOB 3

R8 1k

HA5020 U2
3 IN+
2 IN- OUT 6
1 5

R5 402 R3 402 R4 46.4

HA-5033 U3
4 IN OUT 8

R1 100

-15 R6 15K R60 1K R7 15K +15

C5 .1uF

REF101 U4
6 FEEDBACK RA
5 VOUT 8
2 VTRIM
3 VZ VCC
GND RB
4 1

7 10uF .1uF .001uF +15
C8 C9 C3

R2 38.3k
R11 1.47k

HA5177 U5
3 +IN OUT 6
BAL2
-IN BAL1
2 1 8

HA2-5002 U6
8 IN OUT 4

R66 10

+5A

10uF .1uF .001uF 33pF
C2 C6 C1 C4

HI5700 U8
20 VIN OFW 14
16 CEI D7 2
15 CE2 D6 3
9 3/4R D5 4
23 1/2R D4 5
22 1/4R D3 10
17 VREF+ D2 11
27 VREF- D1 12
CLK D0 13

D7 D6 D5 D4 D3 D2 D1 D0

VREF

FROM CAMERA BNC2 25MHZ R12 10K

HCT161 U7
6 D QD 11
5 C QC 12
4 B QB 13
3 A QA 14
2 CP
7 ENP
10 ENT RCO 15
9 LD
1 CLR

+5A

HCT157 U29
10 B
11 A Y 9
1 SEL
15 OE

MCLK1 BRANCHA1

MCLK2 BRANCHA2

HCT157 U29
3 B
2 A Y 4
1 SEL
15 OE

+5A
1K R50 HCT74
3 CP CLR 1
D Q 5
U34
PR Q 6
4
DEL1 DEL2

1K R70

C150 180pF

MCLK

HCT157 U29
6 B
5 A Y 7
1 SEL
15 OE

BRANCHB1 BRANCHB

BRANCHB2 SEL

+5A R67 10K

133

VIDEO DISPLAY DEMO

CHECKED: B.ROOD	DRAWN: J.SEE
DATE: 1/16/92	PAGE: 3 OF 9
FILENAME: 2DHMU	REV: F

+5D 680

SIP2

680

SIP1 DG

HCT574

8D	8Q
7D	7Q
6D	6Q
5D	5Q
4D	4Q
3D	3Q
2D	2Q
1D	1Q

RM10
RM11
RM12
RM13
RM14
RM15
RM16
RM17

U30

CP
OC

HCT574

U31

CP
OC

HCT574

U32

CP
OC

3D_D0
3D_D1
3D_D2
3D_D3
3D_D4
3D_D5
3D_D6
3D_D7

MCLK

U33
CLK
IN OUT
FCT374

HMU_OFLW

2DC_OFLW

FCT374
IN OUT
CLK

FCT374
IN OUT
CLK

FCT374
IN OUT
CLK

U11
HCT00

U11
HCT00

HCT00
U11

U11
HCT00

R15
340

Q1
TL209

U_FLOW

CLK
IN OUT
FCT374

CLK
IN OUT
FCT374

CLK
IN OUT
FCT374

CLK
IN OUT
FCT374

HCT00
U11

H_SYNCDB

NON-
CONVOLVED

VREF

R43 10K   R62 2K   C12 .1uF

+15

CA3338A
U22

DD0 9 D0
DD1 7 D1   VOUT 12
DD2 8 D2
DD3 5 D3   VREF+ 13
DD4 4 D4   VREF- 11
DD5 3 D5
DD6 6 D6   COMP 14
DD7 1 D7
                  LE   15

MCLK

10uF .1uF .001uF
C10   C15   C11

HA2546
U23

13 VX+   VOUT 1
12 VX-
5   VY+   GAA   16
6   VY-   GAB   14
           GAC   15
9   VZ+
10 VZ-   VYIOA 4
           VYIOB 3
2   VREF

C13 .1uF

R45 1K

R49 15K   R63 1K   R47 15K
-15   +15

+5A
R71 316

74LS123
U24

9 A   Q   5
10 B   Q̄   12
11 CLR
   REXT CEXT
   7   6

R69 5K   C137 150pF

+5A
+5A

74LS123
U24

1 A   Q   13
2 B   Q̄   4
15 CLR
   REXT CEXT
   15   14

R61 25K   R44 1K   C14 .0082uF

+5A
R48 1K

CHANNEL1

+5A
2 16 15

6 IN1+ EN D1 D0
7 IN1-   **U27**
3 IN2+
4 IN2-   OUT 8
11 IN3+
10 IN3-
14 IN4+
13 IN4-
        HA2444

R52 1K   R54 500

R53 500

HA2842
U28
3
2   6

R46 75

BNC7

VREF

10uF .1uF .001uF
C19   C20   C18

CA3338A
U25

3D_D0 9 D0
3D_D1 7 D1   VOUT 12
3D_D2 8 D2
3D_D3 5 D3   VREF+ 13
3D_D4 4 D4   VREF- 11
3D_D5 3 D5
3D_D6 6 D6   COMP 14
3D_D7 1 D7
                  LE   15

MCLK

+15   R58 10K   R65 2K   C17 .1uF

CHANNEL2

HA2546
U26

13 VX+   VOUT 1
12 VX-
5   VY+   GAA   16
6   VY-   GAB   14
           GAC   15
9   VZ+
10 VZ-   VYIOA 4
           VYIOB 3
2   VREF

C16 .1uF

R55 1K

R51 1K
+5A

R56 15K   R64 1K   R57 15K
-15   +15

MCLK

MCLK

A
B

LCEN MODSEL OE

6   40   19

CLK
CLKEN
CLKSEL
+5D

U17

DI0   DO0
DI1   DO1
DI2   DO2
DI3   DO3
DI4   DO4
DI5   DO5
DI6   DO6
DI7   DO7
DI8   DO8
DI9   DO9

D0
D1
D2
D3
D4
D5
D6
D7

H_SYNC
V_SYNC

DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7

H_SYNCD
V_SYNCD

BNC3

R37
75

BNC4

R36
75

DIPSW3   LC0
DIPSW3   LC1
DIPSW3   LC2
DIPSW3   LC3

DIPSW2   LC4
DIPSW2   LC5
DIPSW2   LC6
DIPSW2   LC7

DIPSW1   LC8
DIPSW1   LC9
DIPSW1   LC10

LC0
LC1
LC2
LC3
LC4
LC5
LC6
LC7
LC8
LC9
LC10

HSP9501

20
21
44
43
42
41
26
25
24
23
22

SIP3

10K 10K 10K 10K 10K 10K 10K 10K 10K 10K 10K

+5D

R39 R38

V SYNC OUT TO
FRAME PIN ON 2D

SUBJECT:
VIDEO DISPLAY DEMO

CHECKED: B.ROOD	DRAWN: J.SEE
DATE: 1/16/92	PAGE: 6 OF 7
FILENAME: 9501	REV: F

ALL LED'S ARE TL209

U14 HCT541

| 1 | $\overline{G1}$ |
| 19 | $\overline{G2}$ |

2	A1	Y1	18	R16 340	O2
3	A2	Y2	17	R17 340	O3
4	A3	Y3	16	R18 340	O4
5	A4	Y4	15	R19 340	O5
6	A5	Y5	14	R20 340	O6
7	A6	Y6	13	R21 340	O7
8	A7	Y7	12	R22 340	O8
9	A8	Y8	11	R23 340	O9

2DD0, 2DD1, 2DD2, 2DD3, 2DD4, 2DD5, 2DD6, 2DD7

U15 HCT541

| 1 | $\overline{G1}$ |
| 19 | $\overline{G2}$ |

2	A1	Y1	18	R24 340	O10
3	A2	Y2	17	R25 340	O11
4	A3	Y3	16	R26 340	O12
5	A4	Y4	15	R27 340	O13
6	A5	Y5	14	R28 340	O14
7	A6	Y6	13	R29 340	O15
8	A7	Y7	12	R30 340	O16
9	A8	Y8	11	R31 340	O17

2DD8, 2DD9, 2DD10, 2DD11, 2DD12, 2DD13, 2DD14, 2DD15

U16 HCT541

| 1 | $\overline{G1}$ |
| 19 | $\overline{G2}$ |

2	A1	Y1	18	R32 340	O18
3	A2	Y2	17	R33 340	O19
4	A3	Y3	16	R34 340	O20
5	A4	Y4	15	R35 340	O21
6	A5	Y5	14		H_SYNCDB
7	A6	Y6	13	V_SYNCDB
8	A7	Y7	12	
9	A8	Y8	11	

2DD16, 2DD17, 2DD18, U_FLOW, H_SYNCD, V_SYNCD

BNC5   BNC6

SUBJECT:	
VIDEO DISPLAY DEMO	
CHECKED: B.ROOD	DRAWN: J.SEE
DATE: 1/16/92	PAGE: 7 OF 9
FILENAME: LED	REV: F

FROM COMPUTER

139

J1 1 STROBE
R40
10K
+5D

U18
OC
CP
1D   1Q   19   CIN0
2D   2Q   18   CIN1
3D   3Q   17   CIN2
4D   4Q   16   CIN3
5D   5Q   15   CIN4
6D   6Q   14   CIN5
7D   7Q   13   CIN6
8D   8Q   12   CIN7
HCT574

J1 14 AUTO_LF
SIP4
10K
+5D

U19
OC
CP
1D   1Q   19   CIN8
2D   2Q   18   CIN9
3D   3Q   17   A0
4D   4Q   16   A1
5D   5Q   15   A2
6D   6Q   14
7D   7Q   13
8D   8Q   12
HCT574

J1 17 SLCT_IN
J1 2   DB0
J1 3   DB1
J1 4   DB2
J1 5   DB3
J1 6   DB4
J1 7   DB5
J1 8   DB6
J1 9   DB7
J1 10
J1 20
J1 21
J1 22
J1 23
J1 24
J1 25

10K 10K 10K 10K 10K 10K 10K 10K   R41
10K
SIP4   +5D

HCT574
8D   8Q   12   Y8
7D   7Q   12   Y9
6D   6Q   13   Y10
5D   5Q   14   Y11
4D   4Q   15   Y12
3D   3Q   16   Y13
2D   2Q   17   Y14
1D   1Q   18   Y15
CP   19
OC
U20

U21
1   2
HCT14
J1 16 INIT_PRT
R42
10K
+5D   ID_CS

SUBJECT:
VIDEO DISPLAY DEMO
CHECKED: B.ROOD   DRAWN: J.SEE
DATE: 1/16/92   PAGE: 8 OF 9
FILENAME: PARALLEL   REV: F

U29

+15 >
+5A >
+5D >

B1 B2 B3 B4
C125 C126 C127 C128
150uF 150uF 150uF 150uF

TP1 TP2 JP1

B5
DG >

AG > B6
TP3 TP4 TP5 JP2

U29
OE
SEL
A
B   Y 12
HCT157

U1   U2   U3   U5   U6   U29 U7 PIN 7   PIN 18   PIN 21   PIN 23   PIN 26

+15 C94 C21 C22 C98 C30 C29 C101 C36 C35 C104 C42 C41 C107 C48 C47   +5A C141 C135 C93 C102 C31 C25 C99 C26 C43 C96 C44 C38 C105 C37 C32 C100 C50 C49

AG

-15 C95 C24 C23 C97 C27 C28 C100 C33 C34 C103 C39 C40 C106 C45 C46

AG

(PAGE 2)

U9   U10   U11 U12 U13   +5D U31 U32 U33   U17   U14 U15 U16

+5D C109 C52 C51 C110 C53 C54 C111 C56 C55   C92 C91 C90   C138 C139 C140   +5D C113 C63 C62 C112 C61 C60   +5D C57 C59 C58

DG   DG   DG   DG

(PAGE 3)   (PAGE 4)   (PAGE 6)   (PAGE 7)

U18 U19 U20 U21

+5D C129 C131 C132 C130 C133 C134   +5D C66 C65 C64 C67

DG   DG

(PAGE 8)

U23   U26   U27   U28   U22   U24   U25   +5D

+15 C114 C71 C68 C117 C72 C75 C119 C76 C79 C123 C89 C86   +5A C120 C01 C00 C121 C03 C02 C122 C85 C04   C136

AG   AG   DG

-15 C115 C70 C69 C116 C73 C74 C118 C77 C78 C124 C88 C87

(PAGE 5)

SUBJECT:

VIDEO DISPLAY DEMO

CHECKED: B.ROOD	DRAWN: J.SEE
DATE: 1/16/92	PAGE: 9 OF 9
FILENAME: DECOUPLE	REV: F

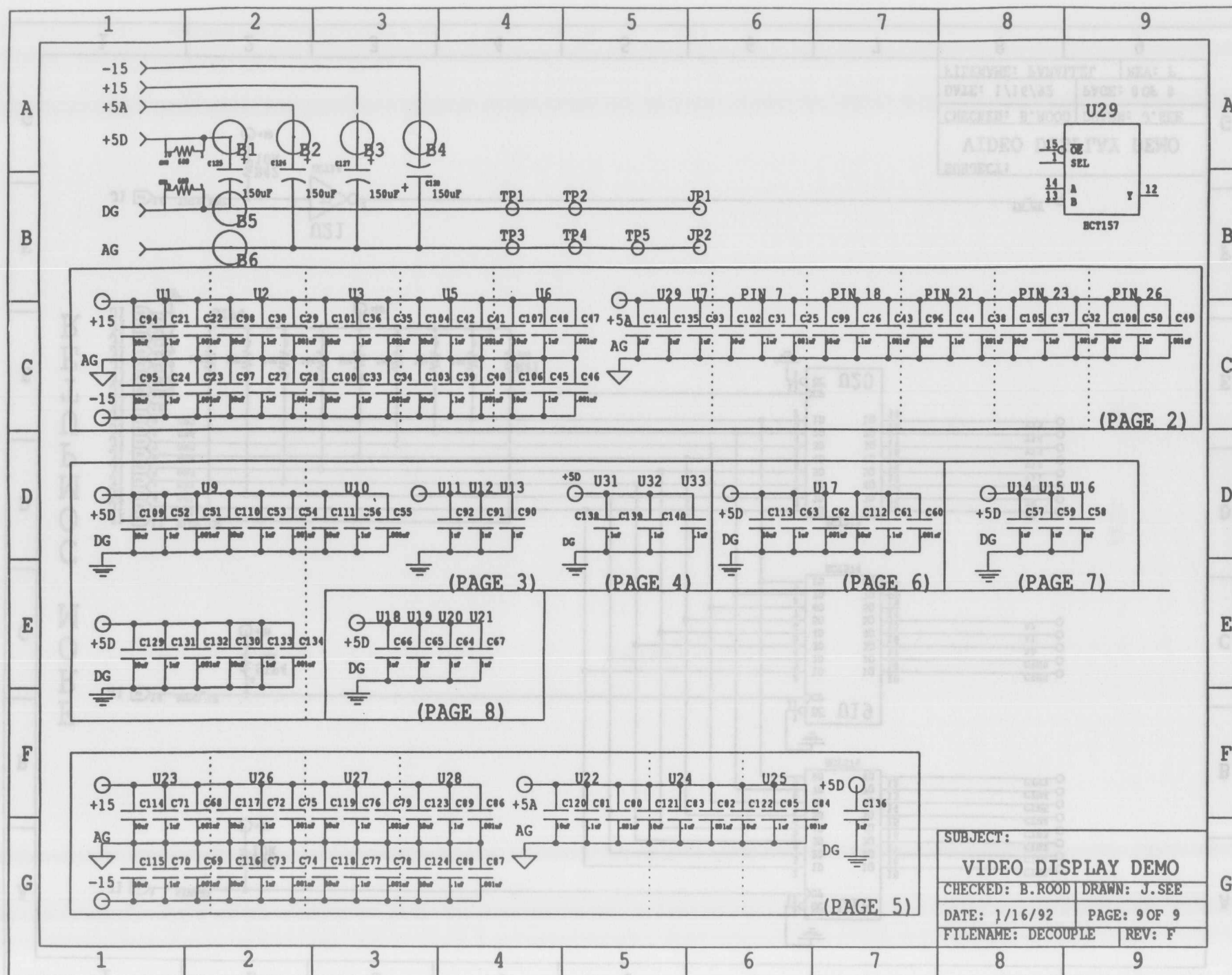| ITEM	QTY	PART-NAME	REFERENCE-DESIGNATOR	DESCRIPTION
1	1	R400	R3	VALUE=400
2	1	R400	R4	VALUE=46.4
3	6	R400	R6 R7 R47 R49 R56 R57	VALUE=15K
4	1	R400	R5	VALUE=402
5	11	R400	R8 R44 R50 R52 R51 R55 R45 R48 R69 R71 R72	VALUE=1K
6	2	R400	R10 R46	VALUE=75
7	13	R400	R9 R12 R13 R37 R38 R39 R36 R41 R42 R40 R43 R58 R67	VALUE=10K
8	1	R400	R11	VALUE=1.47k
9	1	R400	R1	VALUE=100
10	1	R400	R2	VALUE=38.3k
11	2	R400	R14 R68	VALUE=250
12	21	R400	R15 R17 R18 R19 R20 R21 R22 R23 R31 R30 R29 R28 R27 R26 R25 R24 R32 R33 R34 R35 R16	VALUE=350
13	2	R400	R54 R53	VALUE=500
14	1	R400	R70	

15	37	C100	C10 C95 C19 C130	VALUE=10uF
			C2 C96 C97 C98 C99	
			C100 C101 C102	
			C103 C104 C105	
			C106 C107 C108	
			C109 C110 C111	
			C112 C113 C114	
			C115 C116 C117	
			C118 C119 C120	
			C121 C122 C123	
			C124 C94 C129 C8	
16	1	HA3_5033	U3	
17	3	HA1_2546	U23 U1 U26	
18	3	BPOT	R64 R60 R63	VALUE=1K
19	3	BPOT	R65 R62 R59	VALUE=2K
20	1	BPOT	R61	VALUE=25K
21	1	R500	R66	VALUE=10
22	7	BNC	BNC2 BNC1 BNC3	
			BNC6 BNC4 BNC5	
			BNC7	
23	1	HI35700J	U8	
24	1	REF101	U4	
25	1	HA3_5020	U2	
26	1	HA2_5002	U6	
27	2	HT05	U13 U12	
28	1	HA7_5177	U5	
29	2	SIP10	SIP2 SIP1	VALUE=2K
30	2	SIP10	SIP3 SIP4	VALUE=10K
31	1	HMU17J	U10	
32	2	SPDT	SW1 SW2	
33	21	D100	Q1 Q2 Q4 Q5 Q6 Q7	VALUE=TL209
			Q8 Q9 Q17 Q16 Q15	
			Q14 Q13 Q12 Q10	
			Q11 Q19 Q18 Q20	
			Q21 Q3	
34	1	HT161	U7	
35	3	HT541	U16 U14 U15	
36	3	DIPSWA	DIPSW2 DIPSW1	
			DIPSW3	
37	1	HSP9501	U17	

38	31	TP	UC000000 UC000001 UC000002 UC000003 UC000004 UC000005 UC000006 UC000007 UC000008 UC000009 UC000010 UC000011 UC000012 TP3 TP1 TP2 JP1 JP2 TP4 TP5 UC000013 MCLK2 MCLK1 BRANCHA1 BRANCHA2 BRANCHB1 BRANCHB2 DEL2 UC000014 DEL1 UC000015	
39	6	HT574	U19 U30 U31 U20 U18 U32	
40	1	74LS123	U24	
41	2	CA3338AE	U25 U22	
42	1	HA1_2444	U27	
43	1	HA7_2842	U28	
44	6	BANJK	B5 B2 B3 B4 B6 B1	
45	4	C1100	C126 C127 C128 C125	VALUE=150uF
46	38	C200	C3 C1 C11 C18 C22 C23 C25 C28 C29 C32 C34 C35 C38 C40 C41 C43 C46 C47 C49 C51 C54 C55 C60 C62 C68 C69 C74 C75 C78 C79 C80 C82 C84 C86 C87 C134 C132 C142	VALUE=.001uF
47	1	C200	C4	VALUE=33pF
48	43	C200	C5 C6 C9 C7 C13 C15 C17 C16 C12 C20 C21 C24 C26 C27 C30 C31 C33 C36 C37 C39 C42 C44 C45 C48 C50 C52 C53 C56 C61 C63 C70 C71 C72 C73 C76 C77 C81 C83 C85 C88 C89 C133 C131	VALUE=.1uF
49	2	C200	C14 C137	VALUE=.0082uF
50	16	C200	C57 C58 C59 C64 C65 C66 C67 C90 C91 C92 C93 C136 C135 C138 C139 C140	VALUE=1uF

51	2	C200	C141 C150	VALUE=.001
52	1	HT14	U21	
53	1	HT00	U11	
54	1	HT157	U29	
55	1	HSP48908	U9	
56	1	CINCH25	J1	
57	1	HT374	U33	
58	1	HT74	U34	
59	1	D350	D1	

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ADCH Analog-Digital Conversion Handbook, D. H. Sheingold, ed., Prentice-Hall, 1986

ICCCB IC Converter Cookbook, W. G. Jung, H. W. Sams, 1978

HMADB Harris Military Analog Data Book, Harris Semiconductor, 1989

IDB Intersil Data Book, Intersil Inc., 1987

HDADB Harris Data Acquisition Data Book, Harris Semiconductor, 1991

HLTDB Harris Linear and Telecom ICs Data Book, Harris Semiconductor, 1991

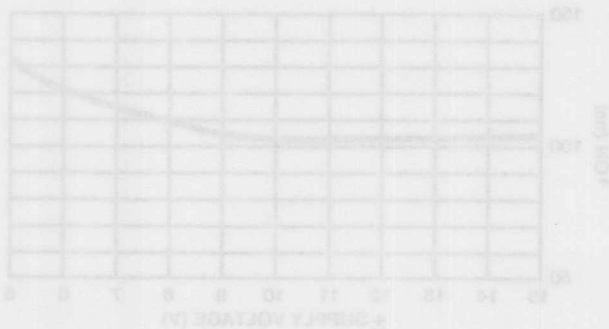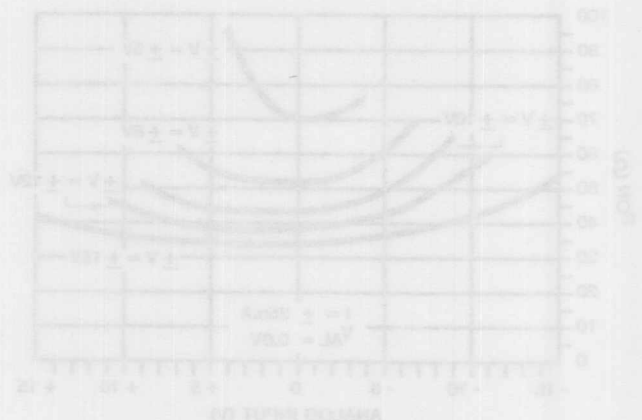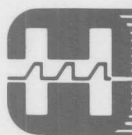# HI-222 VIDEO/HF SWITCH OPTIMIZES KEY PARAMETERS

Author: Brian Alaskiewicz

Introduction

The HI-222 is a dual SPST Analog Switch that compliments the Harris family of high speed op amps and buffers. Although it was specifically designed for use in video routing, this CMOS device is a great choice for all high frequency designs. Through the use of silicon-gate technology and our Dielectric Isolation (DI) process, many key parameters have been enhanced.

With a bandwidth of greater than 200MHz, the HI-222 has the range to satisfy the requirements of present imaging systems, high definition T.V., and even the most sophisticated radar signal conditioning applications. Internal circuitry assures full TTL compatibility over a wide range of supplies and temperatures, while a true "T" Switch design provides optimum off isolation and crosstalk performance. Excellent differential gain and differential phase specifications allow color signals to be transmitted with virtually no degradation. Other typical switch parameters that stand out on the HI-222 include an R_{ON} of 35ohms, T_{ON} of 100ns, T_{OFF} of 75ns, and leakages typically less than 0.5nA.

Reduced Supply Operation

There are many applications where reduced supply operation is preferred. Portable or remote system designers are concerned with low power consumption to extend battery life. Other engineers have only a reduced supply available to use on their boards. In either case, reduced supply operation affects certain parameters. As supply voltage decreases, the on resistance and the switching times increase.

The explanation for these variations can be found in the FET devices comprising the switch cell itself. The variation in on resistance is dependent on the gate-source bias. Since the gate voltage is determined by the supply voltage, the on resistance is a function of the supply voltage.

Switching time is also increased at reduced supply voltages. Figures 1 and 2 show how these two parameters are affected by reduced supply voltages.

The switching thresholds also will shift with supply voltage. For example, with a ± 5.0V supply, the low threshold is reduced to approximately 0.65V and the high threshold to 0.9V. For the HI-222, this means the address level must go below 0.65V to turn the switch on and above 0.9V to disable the switch. This voltage differential of only 0.25V may present a problem in certain applications.

In general, the T_{ON}, R_{ON}, and thresholds of the HI-222 remain relatively consistent down to supply levels of ± 8.0V. The designers who can tolerate these minimal effects on performance will benefit from reduce leakage currents and lower power dissipation.
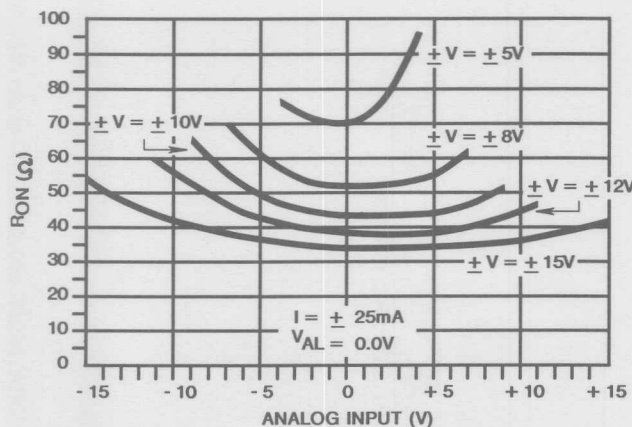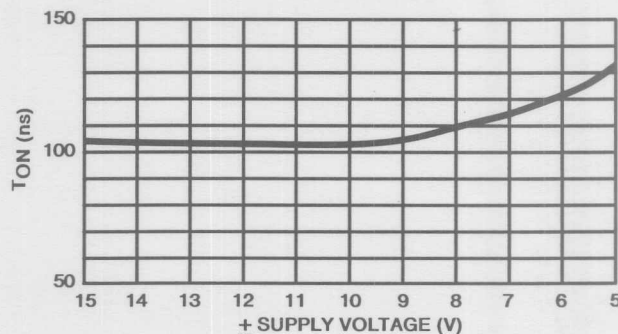

FIGURE 1. R_{ON} vs. ANALOG INPUT vs. SUPPLY

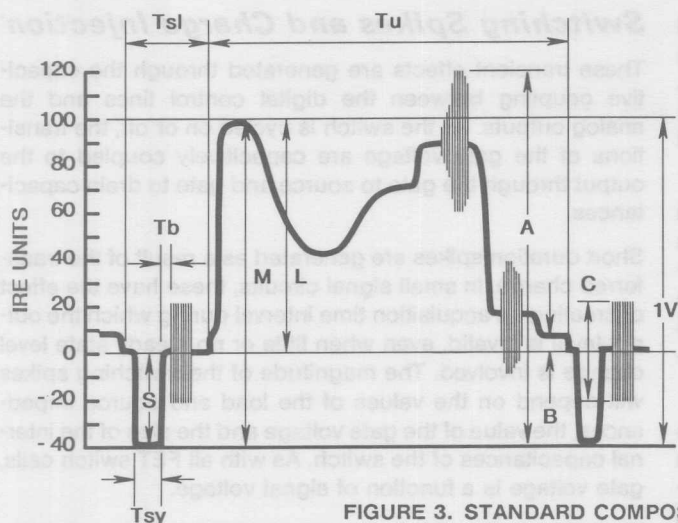

FIGURE 2. SWITCHING TIME vs. SUPPLY

FIGURE 3. STANDARD COMPOSITE COLOR VIDEO SIGNAL

WAVEFORM TERMINOLOGY

A: The peak-to-peak amplitude of the composite color video signal

B: The difference between block level and blanking level (set-up)

C: The peak-to-peak amplitude of the color burst

L: Luminance signal – nominal value

M: Monochrome video signal peak-to-peak amplitude (M = L + S)

S: Synchronizing signal – amplitude

Tb: Duration of breezeway

Tsl: Duration of line blanking period

Tsy: Duration of line synchronizing pulse

Tu: Duration of active line period

Differential Gain and Phase

Two of the most common parameters included in video equipment specifications are differential gain and phase. In video systems, a higher frequency color information signal "rides" on a lower frequency luminance carrier signal. As this luminance, or brightness, amplitude changes, the color signal is subject to changes in gain and phase. These unwanted shifts on the color signal cause the intensity and hue of the color on the display to be misrepresented.

The standard composite color video signal is shown in Figure 3. It consists of a sync pulse and color burst, which occur during a blanking period, and an active line period. The luminance level and color information for an actual video image are transmitted during the active line period. Figure 3 shows two segments of color information being carried at different levels on the luminance signal. The color and hue information is represented as amplitude and frequency variations in the color signal. Differential gain is the change in amplitude of the color signal during changes in luminance level. Likewise, differential phase is the undesired phase shift of the color signal during changes in luminance level.
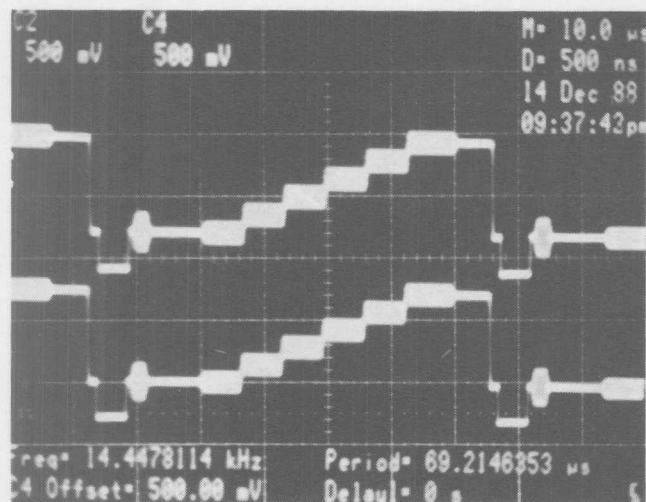
A standard video signal is often used to determine the differential gain and phase of a circuit. Figure 5 shows the NTSC standard test signal at both the input (top view) and output of the HI-222.

There is virtually no visual degradation of the waveform as it is transmitted through the switch. In Figure 6 the output of the HI-222, is overlayed on the input waveform and expanded to further verify that distortion is indeed minimal.
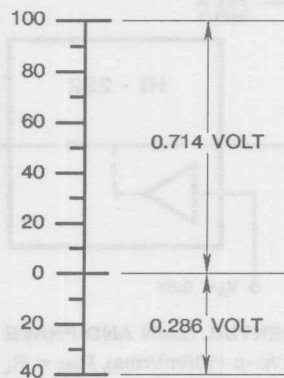

FIGURE 4. THE IRE SCALE UNITS (For 1Vp-p Composite Signal)

FIGURE 5. MTCS STANDARD COLOR VIDEO TEST SIGNAL
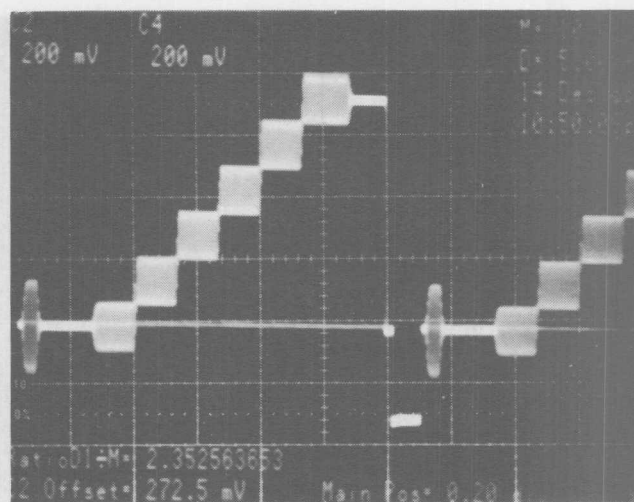AT INPUT AND OUTPUT OF HI-222
(Output at Bottom)

FIGURE 6. INPUT AND OUTPUT OVERLAY OF COLOR
STAIRCASE.

In order to be able to specify the low differential gain and phase of the HI-222, a test technique capable of reading variations of 0.001dB and 0.001 deg. has been developed. An HP 3577A Network Analyzer and an HP 35677A S-Parameter Test Set are used to measure, store, and manipulate waveforms with extreme accuracy.

To simulate the color signal in the standard waveform, an amplitude of 300mVp-p was chosen. This represents a "worse case" amplitude for the color information. A d.c. offset voltage of 1.0V is used to represent a possible full-range shift in luminance level. Figure 3 and the chart in Figure 4 can be used to verify that these levels are sufficient to reproduce the effects of the standard test waveform.

The procedure for testing differential gain and phase is straightforward. The set-up is shown in Figure 7. After the input level and frequency range have been selected, the offset voltage is adjusted to 0.0V. The test is run and inputs A and B are normalized for the 0.0V offset level. The offset is then set to 1.0V. The test is run again and the waveforms of A and B are stored. Waveform A should show the differential gain and phase error at the input caused by the effects of the 1.0V offset. Waveform A is subtracted from waveform B to show the effect of the DUT only, at the output. The results of differential gain and differential phase tests for the HI-222 are shown in Figure 8. The plot shows minimal shifts at the frequencies of interest.
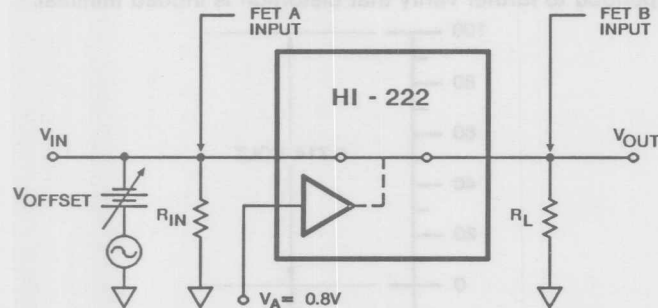
Switching Spikes and Charge Injection

These transient effects are generated through the capacitive coupling between the digital control lines and the analog outputs. As the switch is cycled on or off, the transitions of the gate voltage are capacitively coupled to the output through the gate to source and gate to drain capacitances.

Short duration spikes are generated as a result of the transferred charge. In small signal circuits, these have the effect of creating an acquisition time interval during which the output level is invalid, even when little or no steady state level change is involved. The magnitude of the switching spikes will depend on the values of the load and source impedances, the value of the gate voltage and the size of the internal capacitances of the switch. As with all FET switch cells, gate voltage is a function of signal voltage.

The total net charge injection coupled to the analog circuit is of concern when switching the voltage on a capacitor. In a sample and hold circuit, this injected charge will change the capacitor voltage at the instant the switch is opened. This is caused by the same mechanisms discussed for the small

FIGURE 7. DIFFERENTIAL GAIN AND PHASE TEST CIRCUIT
V_{IN} = 300mVp-p (106mVrms), R_{IN} = R_L = 50Ω,
V_{OFFSET} = 0.0V to 1.0V

$$Q(pC) = C(pf) * V_{OUT} (VOLTS)$$

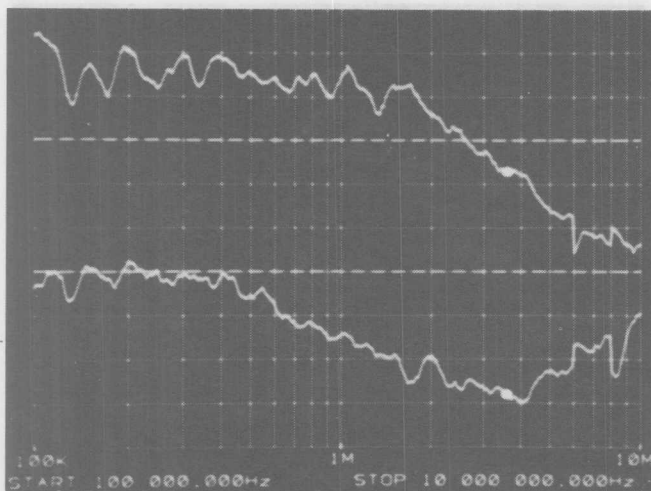$$V = \frac{Q}{C}$$

FIGURE 9. CHARGE INJECTION TEST CIRCUIT

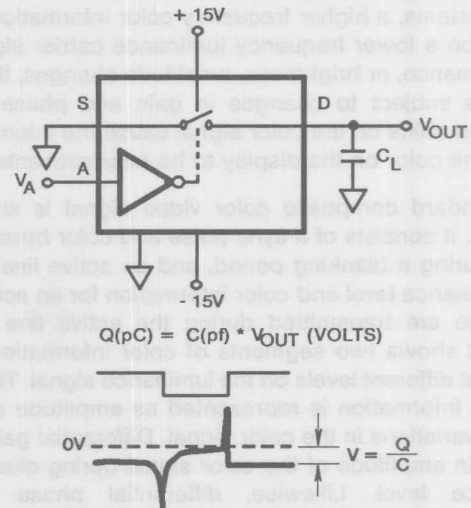FIGURE 8. DIFFERENTIAL GAIN (TOP) AND
DIFFERENTIAL PHASE (BOTTOM)
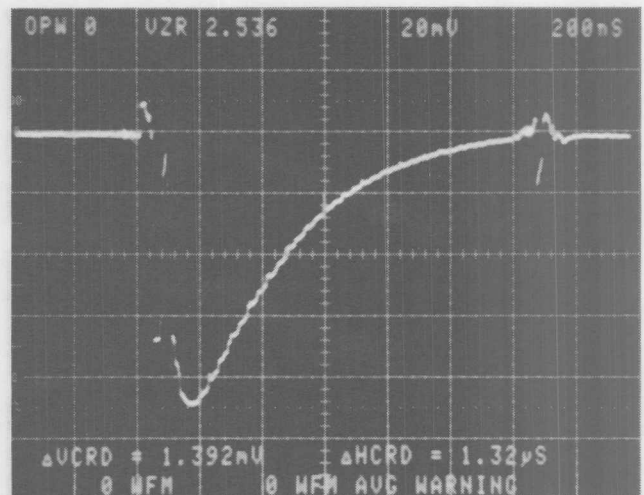(Top = 0.01dB/Div., Bottom = 0.05deg/Div)

FIGURE 10. TYPICAL CHARGE INJECTION WAVEFORM
(CL = 10000pf)

signal application, except in this case the charge is transferred to the hold capacitor creating an offset voltage error. Charge injection is measured in picocoulombs and the voltage transferred to the capacitor computed by V = Charge (pC)/Capacitance (pF).

These effects are considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two sets of switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simultaneously, and their geometries are necessarily different to achieve the desired D.C. resistance match.

Charge injection is measured with the aid of the circuit in Figure 9. The use of an oscilloscope with storage and digital measurement capabilities makes it possible to measure the voltage offset transferred to the capacitor when the switch opens. Figure 10 shows a typical digitized waveform for the HI-222.

The device was addressed at a 500KHz rate with address levels of V_{AL} = 0.8V. and V_{AH} = 2.0V. A 10,000pF capacitor was used on the output. The measured voltage difference from the 0.0V input voltage was 1.392mV. Substituting this information into the formula will yield the charge injection in pC.

$$Q = CV$$
$$= (10,000pF)(1.392 \text{ mV})$$
$$= 13.92pC$$

After characterization of several different diffusion lots of HI-222 devices, it was determined that charge injection varies from lot to lot and from device to device. The majority
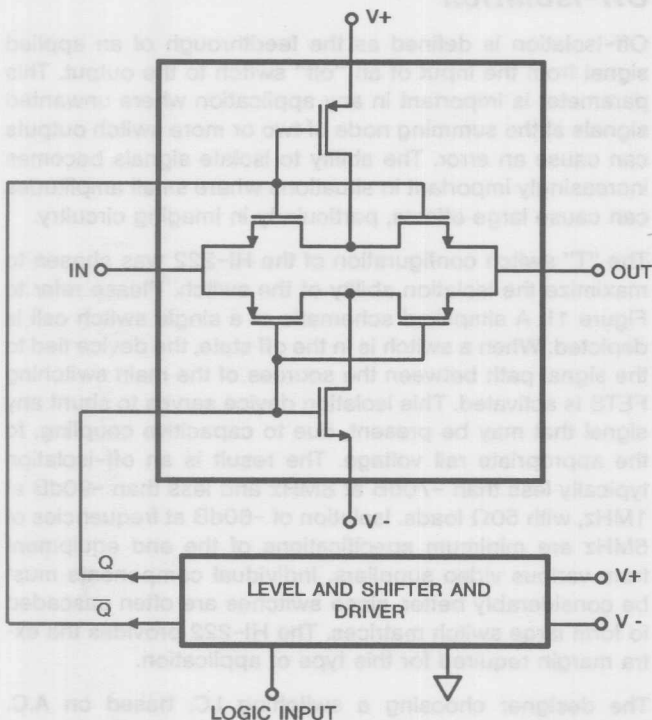
of the devices were in the 30pC to 50pC range, with many exhibiting substantially less transferred charge. The answer to why there is variation can be found in the switch cell itself. The HI-222 uses a "T" switch configuration. Please refer to Figure 11. The slightest process variations can result in small differences in the associated capacitances. The previously discussed differences in the N and P channel geometries, and the fact that six FET devices are being toggled at the same time, also increase the possibility of wafer to wafer variations.

If charge injection is an issue in the application, the question of how to optimize for minimum error arises. Varying one or all of the test conditions results in a change in transferred charge. Changing address levels has the least effect, but an effect none the less. The best address level for the HI-222 is about V_{AH} 2.2V. The single most dramatic change results from adjusting the negative supply to a lower potential. It was found that the charge injection can be totally negated by setting the negative supply to somewhere between −13.0V and −15.0V.

In designs where none of the above changes are feasible, there are compensation schemes that have been proven effective in cancelling charge injection. These methods are based on adding a signal of equal magnitude, but of opposite polarity, to the output in order to cancel the charge injected by the internal capacitances of the switch. One method that works particularly well for the HI-222 is shown in Figure 12. A compensation capacitor approximately equal to the drain capacitance plus the address capacitance is chosen. The 50K potentiometer is used to determine the voltage. At the instant the switch is opened, the charge built up on the compensation capacitor is added at the output of the device. The potentiometer can be adjusted
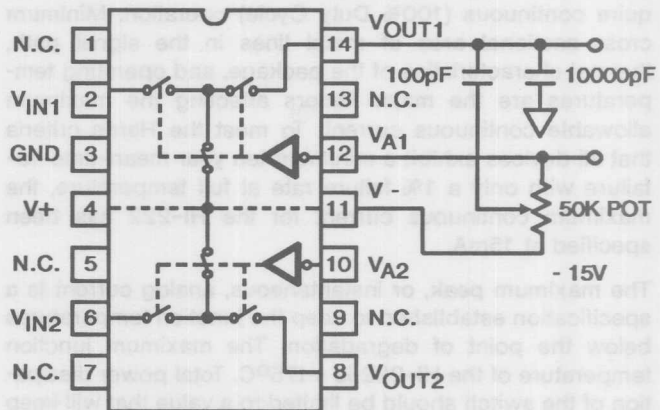

FIGURE 11. SIMPLIFIED SCHEMATIC OF HI-222 SWITCH CELL

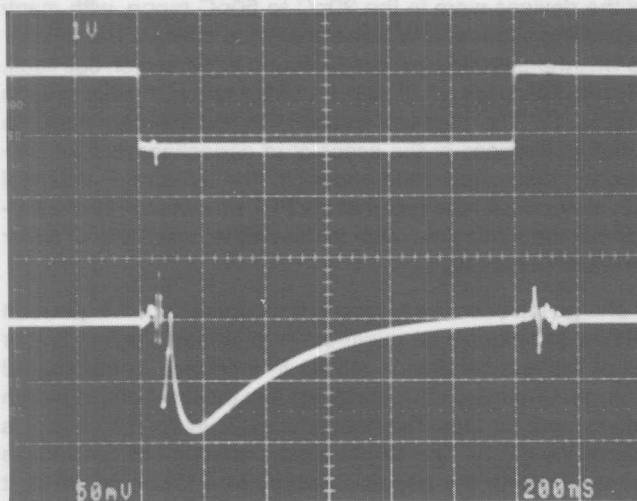FIGURE 12. CHARGE INJECTION COMPENSATION CIRCUIT

FIGURE 13. COMPENSATED CHARGE INJECTION WAVEFORM

to inject the exact amount of compensation charge needed to negate the charge injection of each device. Figure 13 illustrates the typical response of an HI–222 to the conditions specified in Figure 12, showing the switching spikes and the charge injection adjusted to 0.0pC.

Continuous and Peak Analog Current

The maximum analog current is a frequent topic of application discussions. Analog switches are sometimes required to conduct large currents, either continuous or instantaneous, for charging or discharging a capacitance.

The maximum continuous current is the current limit established to ensure reliability for applications which require continuous (100% Duty Cycle) operation. Minimum cross–sectional area of metal lines in the signal path, thermal characteristics of the package, and operating temperatures are the major factors affecting the maximum allowable continuous current. To meet the Harris criteria that all devices exhibit a minimum ten year mean–time–to–failure with only a 1% failure rate at full temperature, the maximum continuous current for the HI–222 has been specified at 15mA.

The maximum peak, or instantaneous, analog current is a specification established to keep the junction temperatures below the point of degradation. The maximum junction temperature of the HI–222 is +175°C. Total power dissipation of the switch should be limited to a value that will keep the junction temperatures below their absolute maximum rating. The maximum amount of power allowable is determined by the maximum junction temperature, the ambient temperature, and the thermal resistance from the die to ambient. It is related by the following equation:

$$P_{MAX} = \frac{T_J - T_A}{\theta_{ja}}$$

The analog current limit for a specific application is determined by the quiescent power dissipation of the device and the maximum total power dissipation allowed. The relationship involves the supply voltages, the R_{ON} of the switch at

the maximum temperature, the supply currents and the total allowable power. The formula for computing the absolute maximum analog current limit is:

$$P_{MAX} = (I_{CC}) (V+ - V-) + (I^2) (R_{ON})$$

A realistic example for the HI–222 might be to find the absolute maximum analog current limit under the following conditions: V+ = +15V, V- = –15V, T_A = +125°C. With these conditions, realistic values might typically be I_{CC} = 2.0mA and R_{ON} = 60Ω. Substitution yields the following:

$$P_{MAX} = \frac{(175 - 125)°C}{75°C/W}$$

$$= 0.667 \text{ W}$$

$$0.667W = (0.002) (30) + (I^2) (60)$$

Solving for I_{MAX}:

$$I_{MAX} = 0.100 = 100mA @ +125°C$$

When power and an input are applied to a device, the junction temperature does not rise instantaneously. The different elements in the thermal path all have thermal capacitance in addition to thermal resistance. Thermal transient response is determined by a time constant which is the product of thermal resistance and capacitance. These parameters vary between package types. Most packages have thermal time constants of at least 200 milliseconds, so that the power pulses of short duration should not raise the junction temperature appreciably. For best reliability, it is recommended that instantaneous current be limited to 80mA and the average power (I^2 x R_{ON}), over any 100 millisecond period, be limited to less than the absolute maximum derated power minus the quiescent power.

Off–Isolation

Off–Isolation is defined as the feedthrough of an applied signal from the input of an "off" switch to the output. This parameter is important in any application where unwanted signals at the summing node of two or more switch outputs can cause an error. The ability to isolate signals becomes increasingly important in situations where small amplitudes can cause large effects, particularly in imaging circuitry.

The "T" switch configuration of the HI–222 was chosen to maximize the isolation ability of the switch. Please refer to Figure 11. A simplified schematic of a single switch cell is depicted. When a switch is in the off state, the device tied to the signal path between the sources of the main switching FETS is activated. This isolation device serves to shunt any signal that may be present, due to capacitive coupling, to the appropriate rail voltage. The result is an off–isolation typically less than –70dB at 8MHz and less than –90dB at 1MHz, with 50Ω loads. Isolation of –60dB at frequencies of 5MHz are minimum specifications of the end equipment from various video suppliers. Individual components must be considerably better, since switches are often cascaded to form large switch matrices. The HI–222 provides the extra margin required for this type of application.

The designer choosing a switching I.C. based on A.C. performance should pay particular attention to the test conditions under which the parameter in question was characterized. Off–isolation, for example, is particularly

susceptible to changes in input amplitude and load resistance. To approximate the signal level used for video tests per accepted NTSC methods, a level of 300mVp-p was chosen and measured at the input of the fixture. The test system included a 50Ω network analyzer, so an R_L of 50Ω was chosen for the fixture. Figure 14 shows typical curves for various loads. Varying supply and address levels has little or no effect on off-isolation performance.

Crosstalk

Crosstalk is the amount of cross coupling from an "off" channel input to an "on" channel output. Although crosstalk can be measured between channels in all possible "on" and "off" configurations, our test condition was chosen to represent the most common application situation. Frequently, in small signal circuitry the major concern is how much unwanted signal is coupled from non-selected inputs to the selected signal path.

The ability of the HI-222 to reject these unwanted signals is greatly improved over common analog switches through the use of the "T" switch design. An explanation of the "T" switch operation can be found in the off-isolation section. This principle improves crosstalk rejection by eliminating unwanted signals from the non-selected signal path.

Another feature of the HI-222 that serves to improve crosstalk rejection is the pin-out of the device. Figure 12 shows the pin functions. With non-connected package pins located between the inputs and outputs of each switch, it is possible to extend a ground shield from the printed circuit board, through the socket pins and lead frame, up to the die itself. It is suggested that all non-connected pins be grounded to achieve this effect.

Figure 15 shows typical crosstalk rejection curves resulting from various load resistances. As with off-isolation, varying supply and address levels has little or no effect on crosstalk rejection.
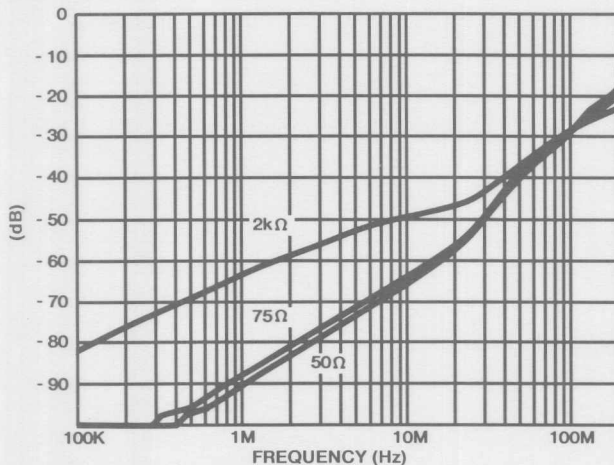
P.C. Board Layout Techniques

The purpose of a P.C. board is to provide circuit devices with an interface to signal sources and outputs, power sources, and external components. Design and construction of P.C. boards for video and high frequency circuitry cannot be taken for granted. Poor techniques can introduce significant errors in A.C. performance.

Use of high quality components alone will not guarantee top performance. Stray capacitance and inductance introduced by line lengths and widths should always be considered. For example, even 1pF of lead capacitance is equivalent to 5KΩ of reactance at 30MHz. This is enough to seriously degrade off-isolation and crosstalk rejection. The following general design rules should eliminate most sources of error and result in good A.C. performance.

- It is especially important that power supply lines have decoupling capacitors to ground permanently installed at the socket pins.

- A ground plane should be used to minimize distributed capacitance.

- All grounds should terminate at a single point ground.

- All sensitive analog lines should be routed between ground traces and kept away from digital lines.

- If Analog and digital lines must cross, they should cross at right angles.

- All unused logic pins should be connected to either V_{AL} or V_{AH}.

- All unused analog input and output pins should be connected to ground.

- Teflon sockets should be used to minimize socket capacitance.
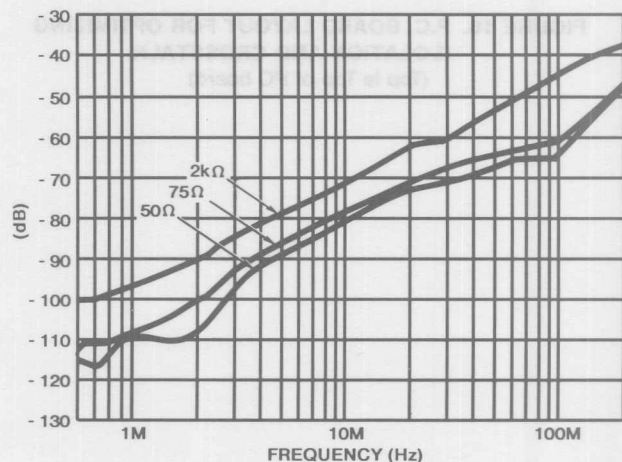
FIGURE 14. OFF-ISOLATION vs. R_L

FIGURE 15. CROSSTALK vs. R_L

In order to optimize the A.C. parameters at high frequencies, a few of the above rules were taken one step further. Input and output connectors should be located as close as physically possible to the device to minimize lead capacitance. Regarding actual board layout, techniques similar to those shown in Figure 16 are recommended. The functional pin-

out of the device is used to its greatest advantage by placing ground lands in every available space and actually over the lands of non-connected pins. If sockets are employed, the pin to pin capacitance can be greatly reduced by using gold pins with all plastic spacing material removed. The single most effective option for enhancing isolation between socket pins is the use of a shielding barrier. This can be constructed from either P.C. board material or copper foil that is soldered to the ground plane and reaches up to contact the underside of the device. The barrier should run lengthwise down the center and extend slightly beyond the ends of the device.

Conclusion

The Harris HI-222 is an extremely fast monolithic CMOS analog switch designed specifically for imaging and HF applications. Key parameters were not compromised to achieve the excellent bandwidth and isolation characteristics of this versatile device.

Acknowledgements

Special thanks goes to Greg Williams for his extensive technical assistance and to Randy Heilman for sharing his design expertise.

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1) Don Jones and Al Little, "CMOS Analog Multiplexers and Switches; Application Considerations", Harris Application Note #520.

2) Carl Wolfe, "Common Questions Concerning CMOS Analog Switches", Harris Application Note #532.

3) Brian Mathews, "Recommended Test Procedures for Analog Switches", Harris Application Note #557.

4) L.E. Weaver, Television Video Transmission Measurements, London, Ebenezer Baylis and Son Ltd, 1979.
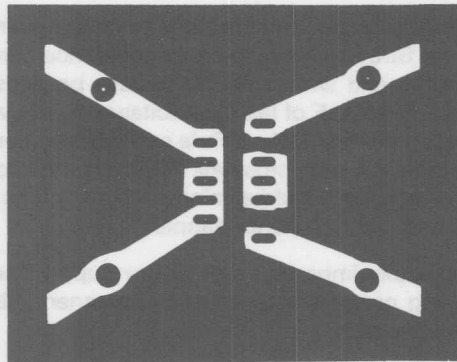
TOP
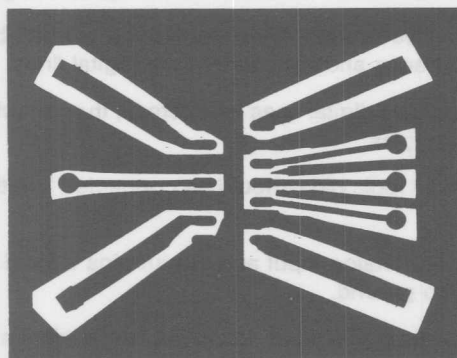
BOTTOM

FIGURE 16. P.C. BOARD LAYOUT FOR OPTIMIZING ISOLATION AND CROSSTALK
(Top is Top of PC board)